ECE 145C / 218C, notes set xx: PLLs and Synthesizers

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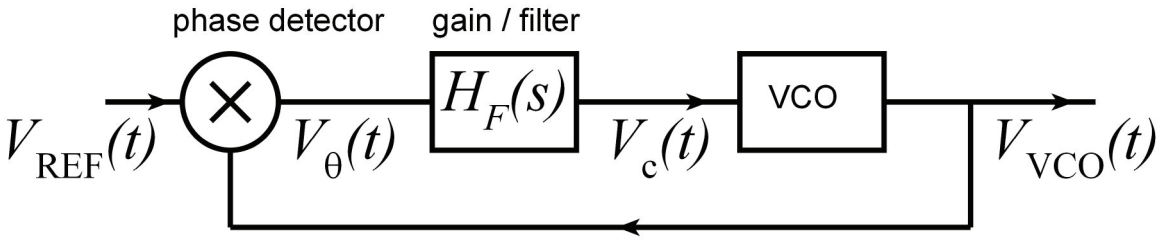
Elementary Phase Lock Loop

Loop consists of :

Phase detector

Loop filter

Voltage controlled oscillator



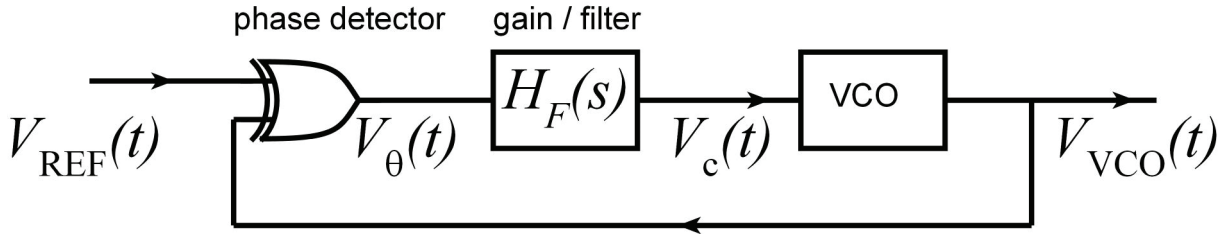
Loop operation:

detector measures phase difference of VCO and reference

phase error signal amplified and filtered.

error signal adjusts VCO phase and frequency.

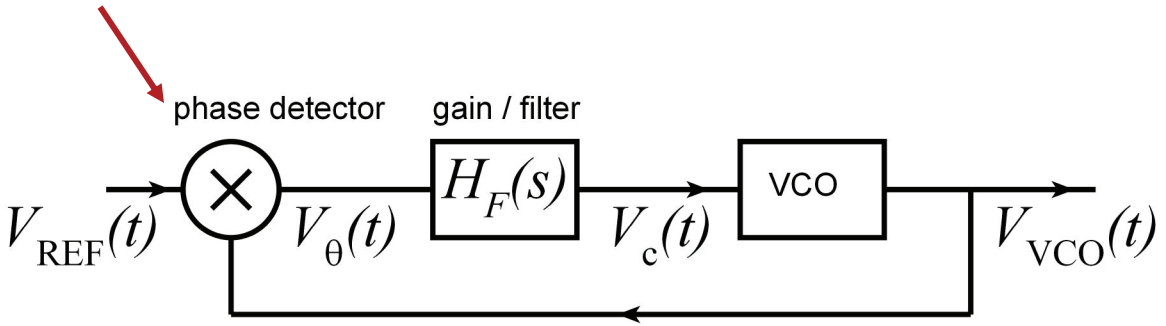
with good design / luck, VCO phase tracks that of reference



Mixer as Phase Detector

$$V_{RF}(t) = V_{RF}\cos(\omega_{RF}t + \theta_{RF}) \qquad V_{VCO}(t) = V_{VCO}\sin(\omega_{VCO}t + \theta_{VCO})$$

$$\Delta\omega = \omega_{VCO} - \omega_{RF}\,;\ \Delta\theta = \theta_{VCO} - \theta_{RF}$$



Idealized mixer:

$$V_\theta(t) = V_{RF}(t)V_{VCO}(t)/V_x$$
$$= (V_{RF}V_{VCO}/V_x)\left(\sin(\Delta\omega\cdot t + \Delta\theta\right) + \text{term at } (\omega_{RF} + \omega_{VCO})$$

Real mixer:

$$V_\theta(t) = A_{mixer}\cdot V_{RF}(t)\cdot\frac{V_{VCO}(t)}{\|V_{VCO}(t)\|}$$
$$= A_{mixer}\cdot V_{RF}\left(\sin(\Delta\omega\cdot t + \Delta\theta\right) + \text{terms at } (\omega_{RF} + N\omega_{VCO})$$

If $\Delta\omega = 0 \rightarrow$ Phase detector $\rightarrow \quad V_\theta(t) = A_{mixer}\cdot V_{RF}\sin\left(\Delta\theta\right) = K_{pd}\sin\left(\Delta\theta\right)$

For small $\Delta\theta$, $\quad V_\theta(t) = K_{pd}\left(\Delta\theta\right)$

XOR Gate as Phase Detector

$V_{RF}(t) = +1, -1, +1, -1, \ldots$

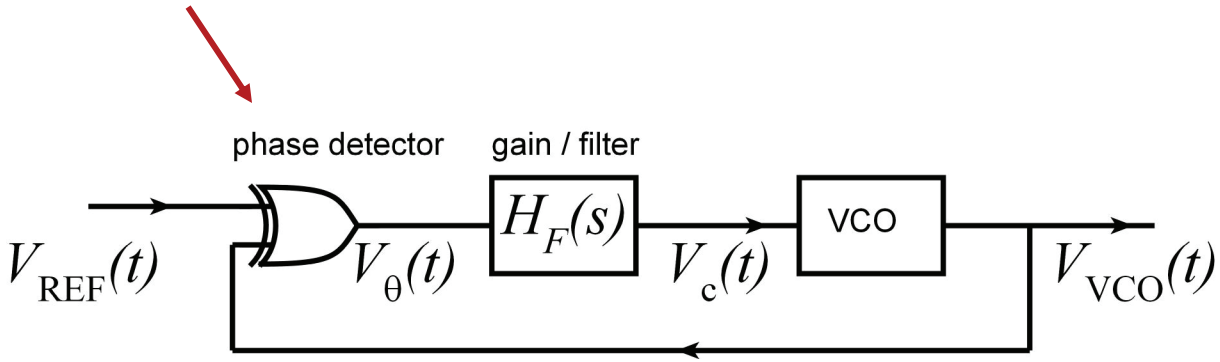
squarewave (binary sequence), frequency ω_{RF}, Phase θ_{RF}

$V_{VCO}(t) = +1, -1, +1, -1, \ldots$

squarewave, frequency ω_{LO}, Phase θ_{LO}

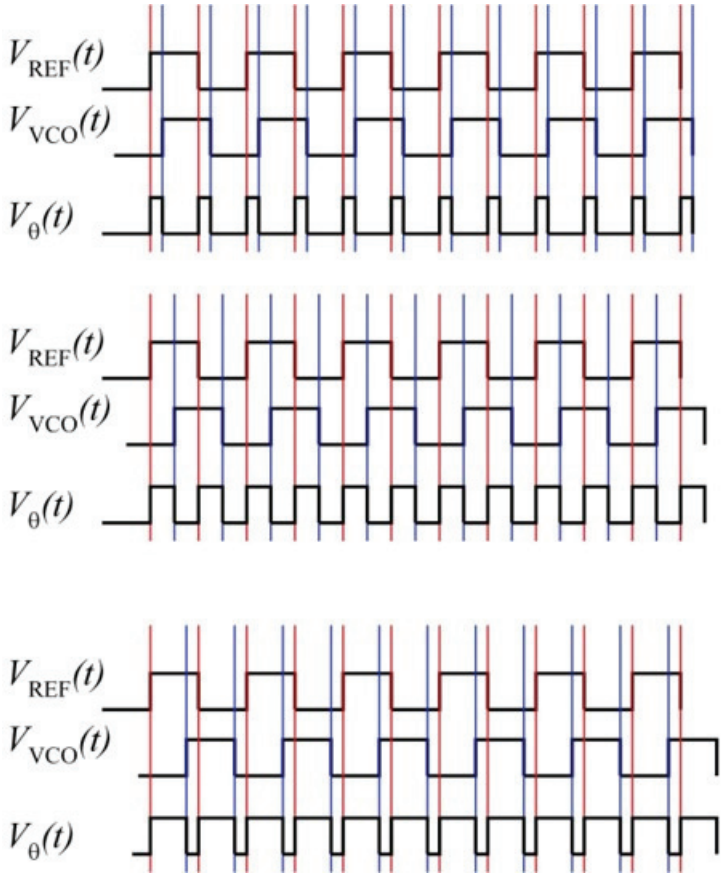
XOR Gate :

$V_{\theta}(t) = V_{RF}(t) \otimes V_{VCO}(t)$

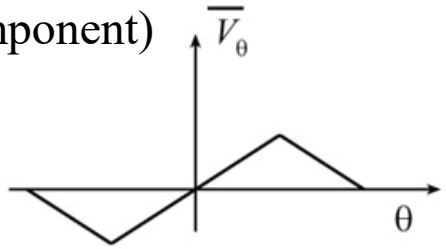


XOR Gate as Phase Detector

Linear voltage-phase characteristics
if signal period is long
compared to
logic gate switching times.



(DC component)



VCO Characteristics

VCO Frequency: $\omega_{\text{VCO}}(t) = \omega_0 + K_{VCO}V_C(t)$

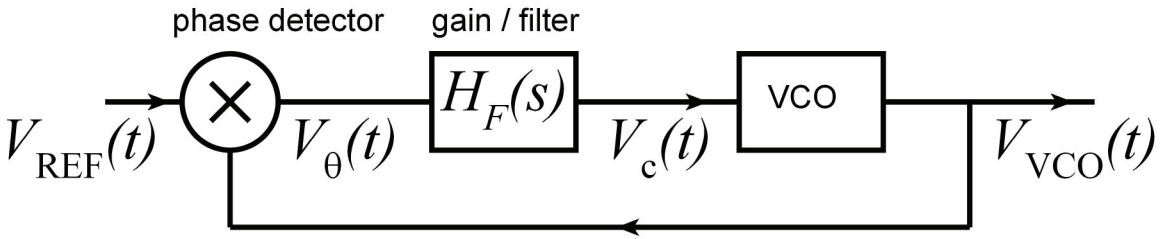
K_{VCO} : rad/sec/volt

Taking the deviation relative to that of ω_0, the VCO phase is

$$\theta_{\text{VCO}}(t) = K_{VCO}\int V_C(t)dt$$

In the LaPlace domain:

$$\theta_{\text{VCO}}(s) = K_{VCO}V_C(s)/s$$

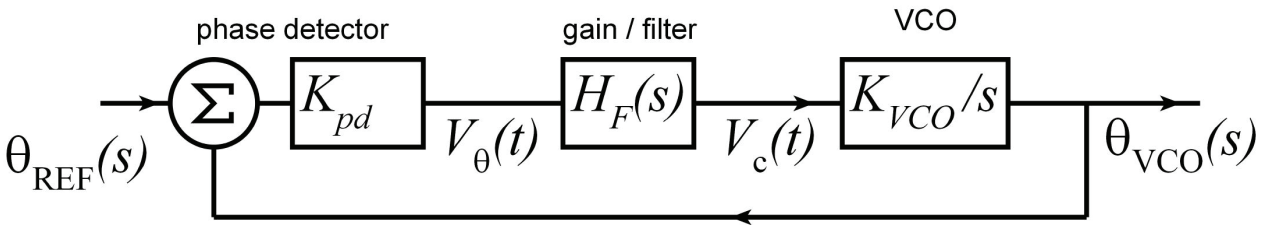


Loop Transmission, loop transfer function

Phase detector : $V_\theta = K_{pd}(\theta_R - \theta_{VCO})$

Loop Filter: $H_F(s)$

VCO: $\theta_{\mathrm{VCO}}(s) = K_{VCO}V_C(s)/s$



Feedback loop transmission:

$T(s) = K_{pd}H_F(s)K_{VCO}/s$

Phase Transfer function

$$\frac{\theta_{VCO}(s)}{\theta_{REF}(s)} = \frac{T(s)}{1+T(s)}$$

Design of $T(s)$ follows standard feedback loop theory

Loop Transmission, loop transfer function

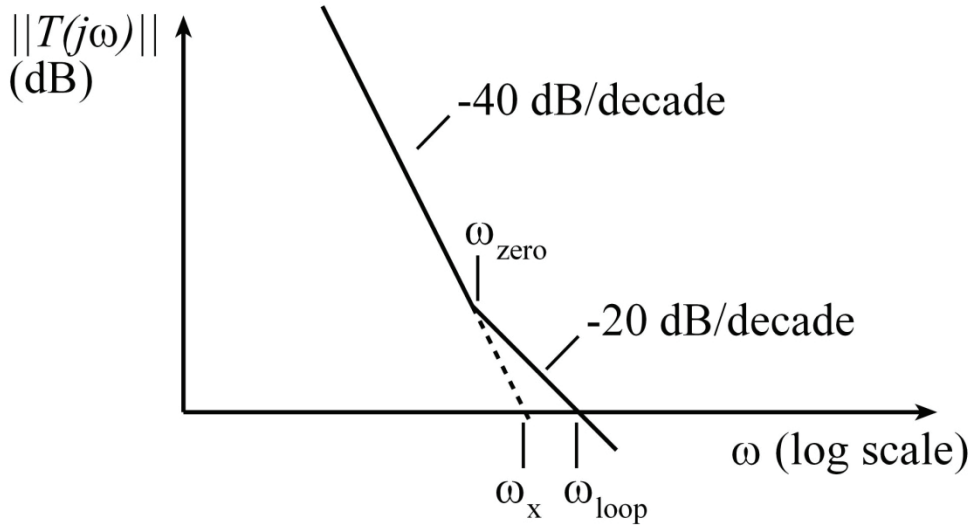
Assume Loop Filter is integrator
with compensating zero:

$$H_F(s) = (1 + s\tau_z) / s\tau_i$$

Loop Transmission:

$$T(s) = \frac{K_{pd} H_F(s) K_{VCO}}{s} = \frac{K_{pd} K_{VCO}(1 + s\tau_z)}{s^2 \tau_i} = \left(\frac{\omega_x}{s}\right)^2 \cdot (1 + s / \omega_{zero})$$

$T(s)$ deceases at -40 dB/decade,
would cross through 0dB @ ω_x.



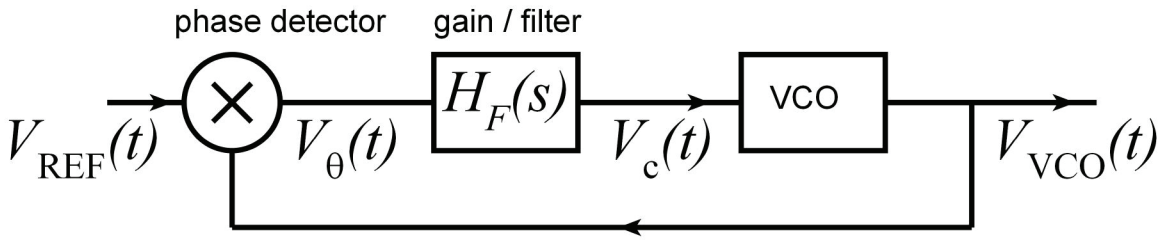
The compensating zero (typically ~50% of ω_{loop})
increases phase margin,
..and increases the loop bandwidth ω_{loop} to somewhat above ω_x.

Why Use loop integrator ? To avoid static phase error !

Suppose we did not use a loop integrator

$H_F(s) = H_0$

and $T(s) = \dfrac{K_{pd} H_0 K_{VCO}}{s}$



VCO frequency: $\omega_{VCO} = \omega_0 + K_{VCO} V_C$

$\rightarrow V_C = (\omega_{VCO} - \omega_0) / K_{VCO}$ and $V_\theta = (\omega_{VCO} - \omega_0) / K_{pd} H_0$

$\rightarrow \theta_{Ref} - \theta_{VCO} = (\omega_{VCO} - \omega_0) / K_{pd} H_0 K_{VCO}$

As we tune the VCO frequency, the phase of the VCO deviates from that of the reference $\rightarrow$ phase error.

Static phase error is avoided by making $H_f(s)$ infinite at DC.

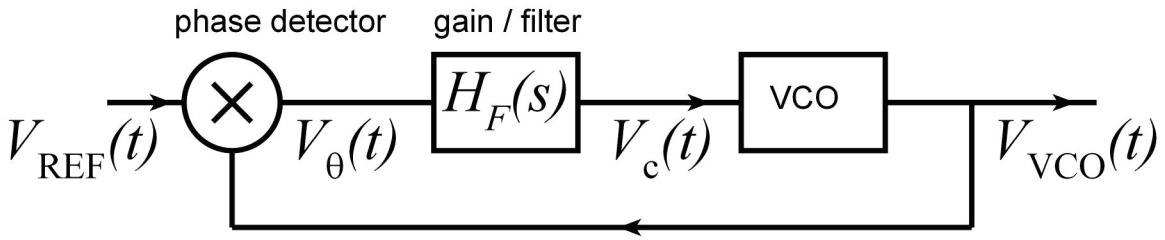
Phase Error With Frequency Ramp

Assume a loop integrator

$$H_F(s) = (1+s\tau_z)/s\tau_i \xrightarrow{\text{at low frequencies}} 1/s\tau_i$$

$$T(s) = \frac{K_{pd}K_{VCO}(1+s\tau_z)}{s^2\tau_i} = \left(\frac{\omega_x}{s}\right)^2 \cdot (1+s/\omega_{zero})$$

VCO frequency: $\omega_{\text{VCO}} = \omega_0 + K_{VCO}V_C$



PLLs used in synthesizers are often used to scan signal frequencies,

i.e. to generate a frequency chirp: $d\omega_{\text{VCO}}/dt = \text{constant}$.

$$\rightarrow (dV_C/dt) = (d\omega_{\text{VCO}}/dt)/K_{VCO}$$

The loop filter is an integrator: $V_\theta \cong \tau_i(dV_C/dt) = (d\omega_{\text{VCO}}/dt)(\tau_i/K_{VCO})$

$$\rightarrow \theta_{\text{Ref}} - \theta_{VCO} = (d\omega_{\text{VCO}}/dt)(\tau_i/K_{VCO}K_{pd})$$

A fixed frequency scan rate causes a fixed phase deviation of the VCO from

that of the reference → *ramp* phase error.

Ramp phase error can be avoided by adding another integrator and compensating zero to $H_f(s)$.

PLL Slew Rate.

Given a finite frequency scan rate $d\omega_{\text{VCO}} / dt = \text{constant}$.

$(dV_C / dt) = (d\omega_{\text{VCO}} / dt) / K_{VCO}$

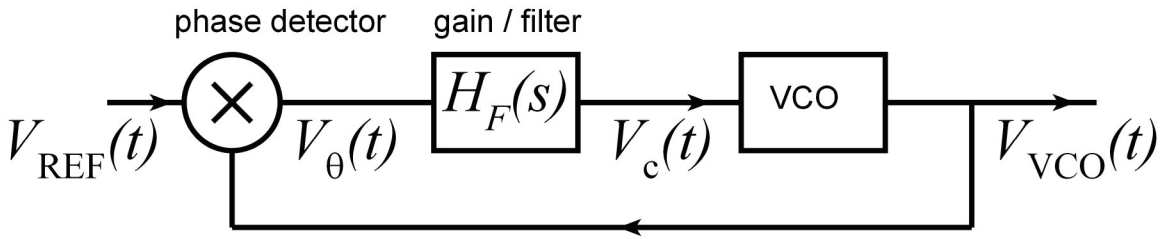
The loop filter is an integrator: $V_\theta \cong \tau_i (dV_C / dt) = (d\omega_{\text{VCO}} / dt)(\tau_i / K_{VCO})$

In the last page, we had assumed $V_\theta(t) = K_{pd}(\Delta\theta)$.

This gave $\theta_{\text{Ref}} - \theta_{VCO} = (d\omega_{\text{VCO}} / dt)(\tau_i / K_{VCO} K_{pd})$.

If the phase detector has sinusoidal characteristics: $V_\theta(t) = K_{pd} \sin(\Delta\theta)$

Then the maximum range of V_θ is $\pm K_{pd}$



Maximum Frequency scan rate.

$\| d\omega_{\text{VCO}} / dt \|_{\max} = K_{VCO} K_{pd} / \tau_i = \omega_x^2$

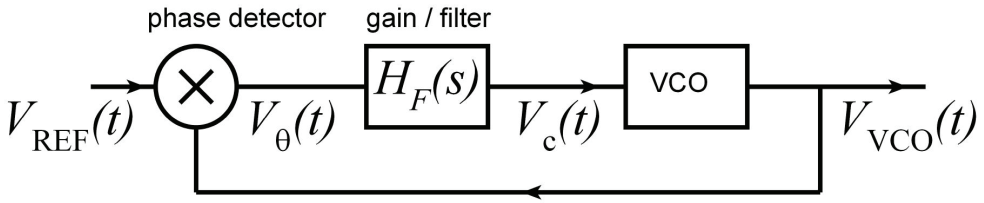
Fast frequency scanning is important in some synthesizer applications.

For faster slew rate, add to the phase detector a counter that counts up on $V_{\text{Ref}}(t)$ transitions and down on $V_{VCO}(t)$ transitions.

Maximum measurable phase range is then the maximum numerical count times 360 degrees.

Maximum Loop Acquisition Bandwidth

If V_{REF} is at frequency ω_{REF},
and V_{VCO} is at frequency ω_{VCO},
then V_θ, the output of the phase detector,
is at frequency $\pm(\omega_{\text{REF}} - \omega_{\text{VCO}})$.



If this frequency is much greater than the loop bandwidth ω_{loop},
then the loop will not respond; no significant error signal is generated
to bring the VCO into lock with the reference.

PLLs will not acquire lock if $(\omega_{\text{REF}} - \omega_{\text{VCO}})$ is more than a few times ω_{loop}.

Even approximate analysis of loop capture dynamics is complex,
and beyond our scope.

Vector Signal Representation: the (I,Q) plane

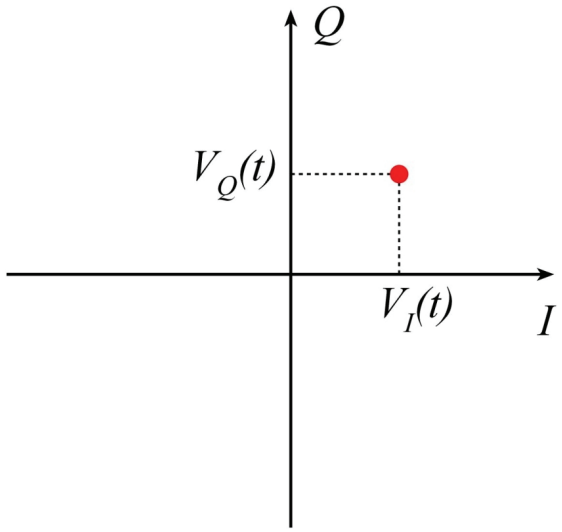
$$V_{RF}(t) = \mathrm{Re}\left\{\left(V_I(t) + jV_Q(t)\right)\cdot e^{j\omega_{RF}t}\right\}$$

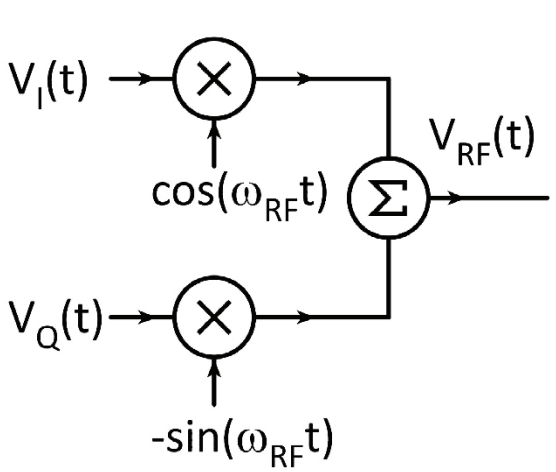
$$= \mathrm{Re}\left\{\left(V_I(t) + jV_Q(t)\right)\cdot\left(\cos(\omega_{RF}t) + j\sin(\omega_{RF}t)\right)\right\}$$

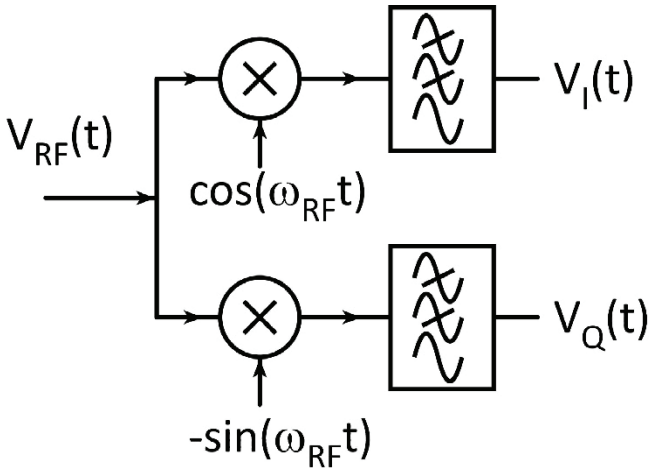
$$= \mathrm{Re}\begin{Bmatrix} V_I(t)\cos(\omega_{RF}t) - V_Q(t)\sin(\omega_{RF}t) \\ +jV_I(t)\sin(\omega_{RF}t) + jV_Q(t)\cos(\omega_{RF}t)\end{Bmatrix}$$

$$= V_I(t)\cos(\omega_{RF}t) - V_Q(t)\sin(\omega_{RF}t)$$

note the "−" sign



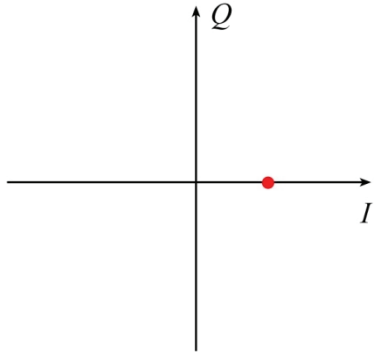




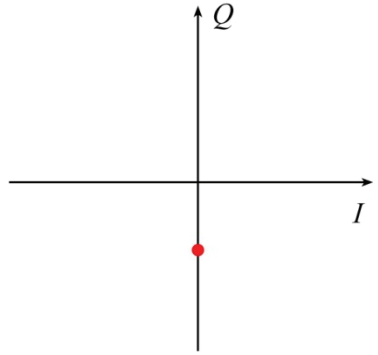
IQ Signal Representation

$$V_{RF}(t) = V_I(t) \cdot \cos(\omega_{RF} t) - V_Q(t) \cdot \sin(\omega_{RF} t)$$

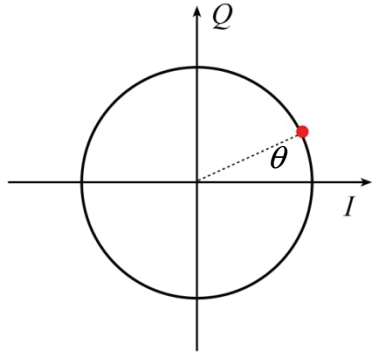
cosine wave



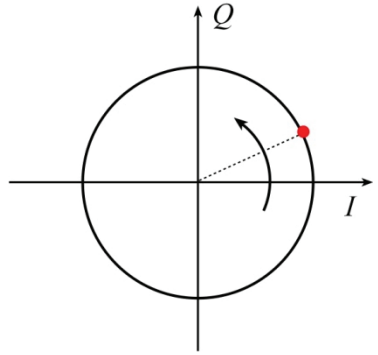
sine wave



$\cos(\omega_{RF} t + \theta)$



$\cos(\omega_{RF} t + \Delta\omega t)$



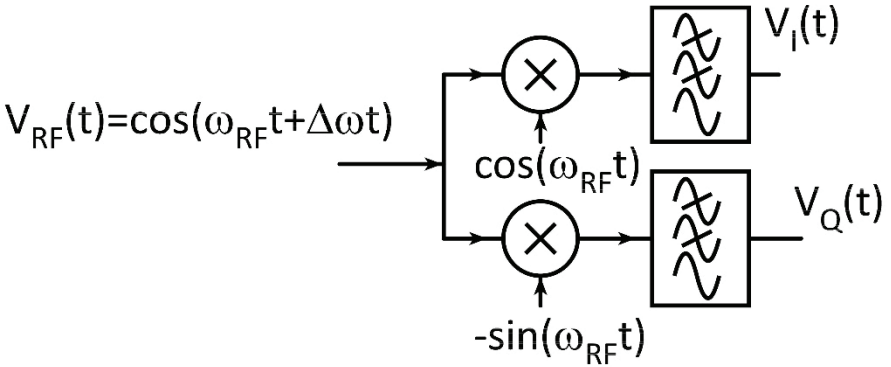
spins counter - clockwise at angular frequency $\Delta\omega$

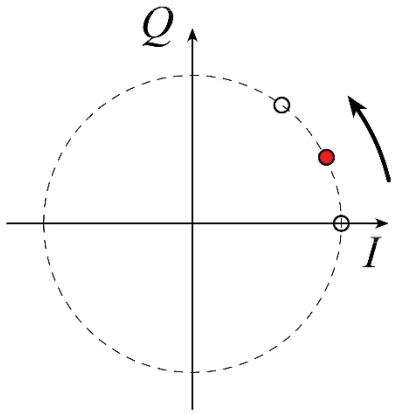
Frequency difference detector (1)

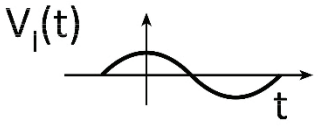
Consider case of nonzero frequency difference

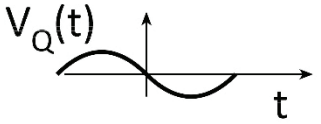
$$V_I(t) = 2K_1 \cos(\omega_{RF}t + \Delta\omega t)\cos(\omega_{RF}t)$$
$$= K_1 \cos(\Delta\omega t) + \text{ term at } 2\omega_{RF}$$

$$V_Q(t) = -2K_1 \cos(\omega_{RF}t + \Delta\omega t)\sin(\omega_{RF}t)$$
$$= K_1 \sin(\Delta\omega t) + \text{ term at } 2\omega_{RF}$$









$$4j\cos(A)\sin(B) = (z_A + 1/z_A)(z_B - 1/z_B)$$
$$= z_A z_B - 1/z_A z_B + z_B/z_A - z_A/z_B$$
$$= 2j\sin(A+B) - 2j\sin(A-B)$$
$$2\cos(A)\sin(B) = \sin(A+B) - \sin(A-B)$$

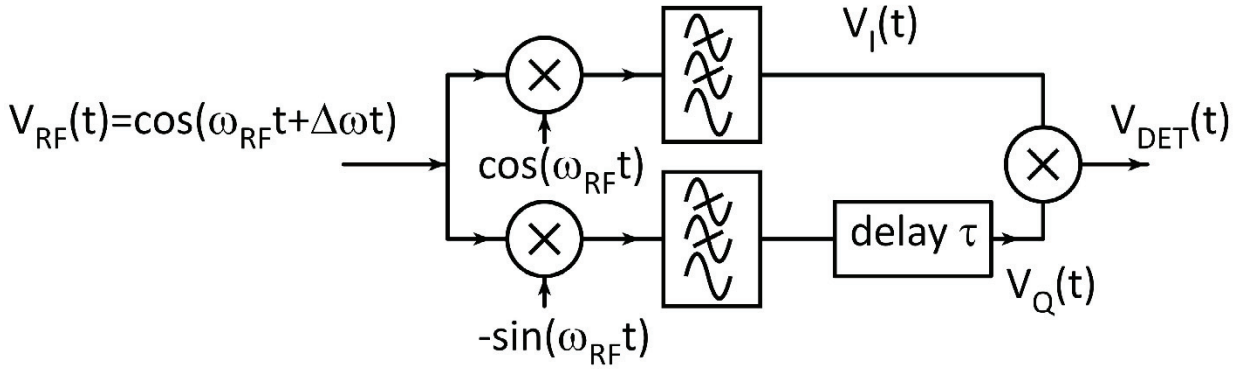
Frequency difference detector (2)

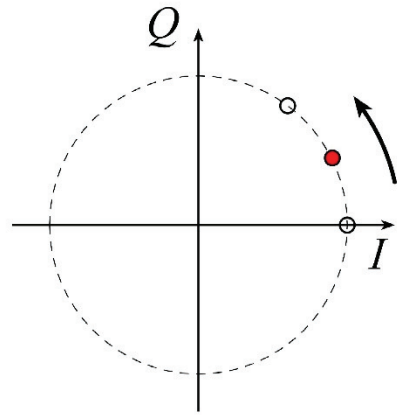
$$V_I(t) = K_1 \cos(\Delta\omega t)$$
$$V_Q(t) = K_1 \sin(\Delta\omega(t-\tau)) = K_1 \sin(\Delta\omega t - \Delta\omega\tau)$$

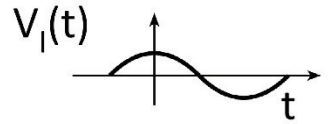
$$V_{DET}(t) = K_3 V_I(t) V_Q(t)$$
$$= K_1 K_3 \cos(\Delta\omega t)\sin(\Delta\omega t - \Delta\omega\tau)$$
$$= (K_1 K_3 / 2)\sin(\Delta\omega\cdot\tau) + (K_1 K_3 / 2)\sin(2\Delta\omega t)$$

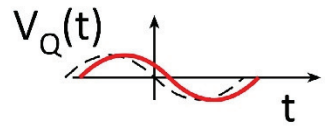
DC output voltage proportional to frequency difference

This voltage, if large enough, will force loop to lock









$$4j\cos(A)\sin(B) = (z_A + 1/z_A)(z_B - 1/z_B)$$
$$= z_A z_B - 1/z_A z_B + z_B/z_A - z_A/z_B$$
$$= 2j\sin(A+B) - 2j\sin(A-B)$$
$$2\cos(A)\sin(B) = \sin(A+B) - \sin(A-B)$$

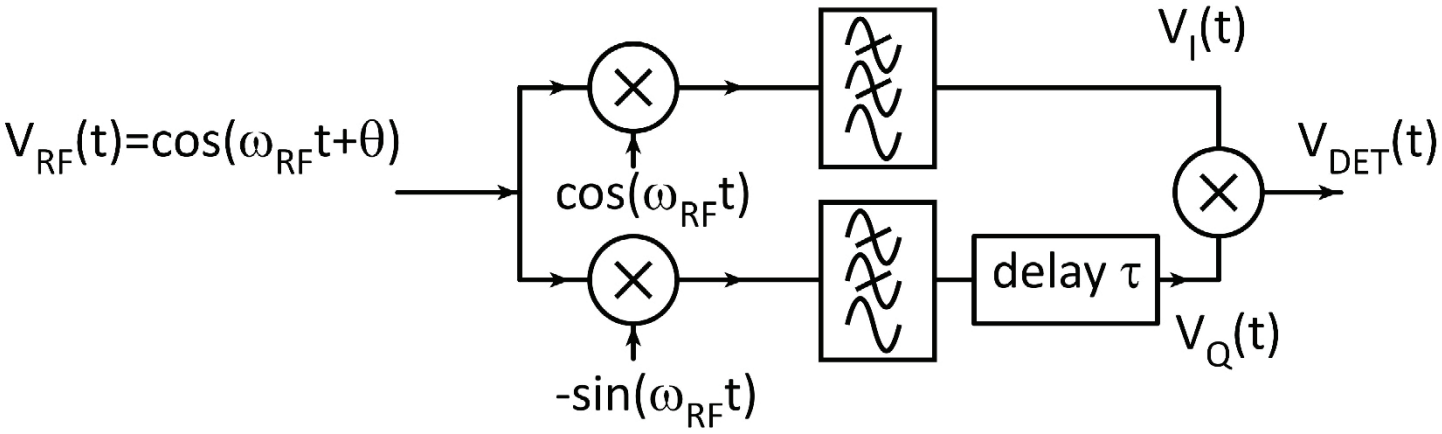
Frequency difference detector (3)

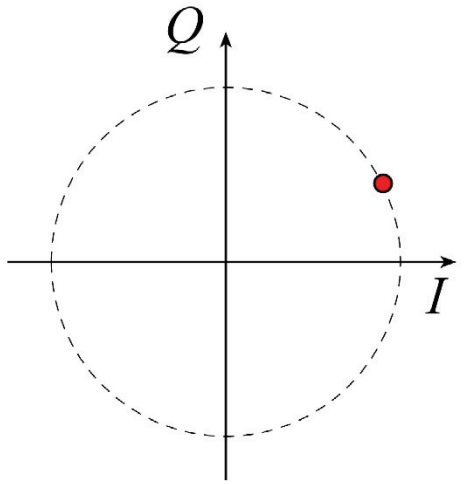
Consider instead: zero frequency difference, nonzero phase difference

$$V_I(t) = K_1 \cos(\theta)$$
$$V_Q(t) = K_1 \sin(\theta)$$

$$V_{DET}(t) = K_3 V_I V_Q$$
$$= K_1 K_3 \cos(\theta)\sin(\theta)$$
$$= (K_1 K_3 / 2)\sin(2\theta) + (K_1 K_3 / 2)\sin(\theta - \theta)$$

$$V_{DET}(t) = (K_1 K_3 / 2)\sin(2\theta)$$





DC output voltage proportional to sine of *twice the phase difference*

"PFD"="phase-frequency difference detector"

$$4j\cos(A)\sin(B) = (z_A + 1/z_A)(z_B - 1/z_B)$$
$$= z_A z_B - 1/z_A z_B + z_B/z_A - z_A/z_B$$
$$= 2j\sin(A+B) - 2j\sin(A-B)$$
$$2\cos(A)\sin(B) = \sin(A+B) - \sin(A-B)$$

Clock and data recoverey in communications receivers

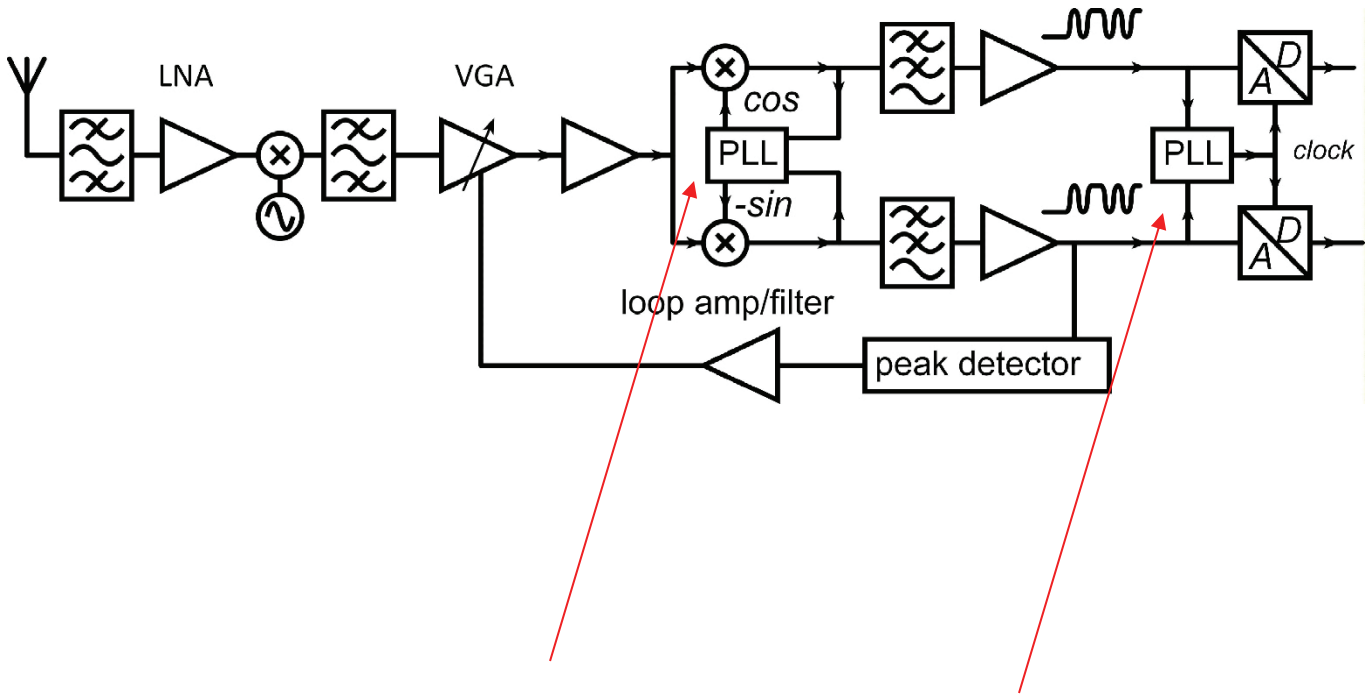
Here is a (rough) block diagram of a communications receiver.

The first VCO can be free-running...

The 2nd must be phase-locked to the IF carrier
(or the RF carrier if direct conversion)

We need a 2nd PLL to sychronize to the data symbol period.

A simple PLL will not work for either of these.



Simple PLL's don't work with modulated data

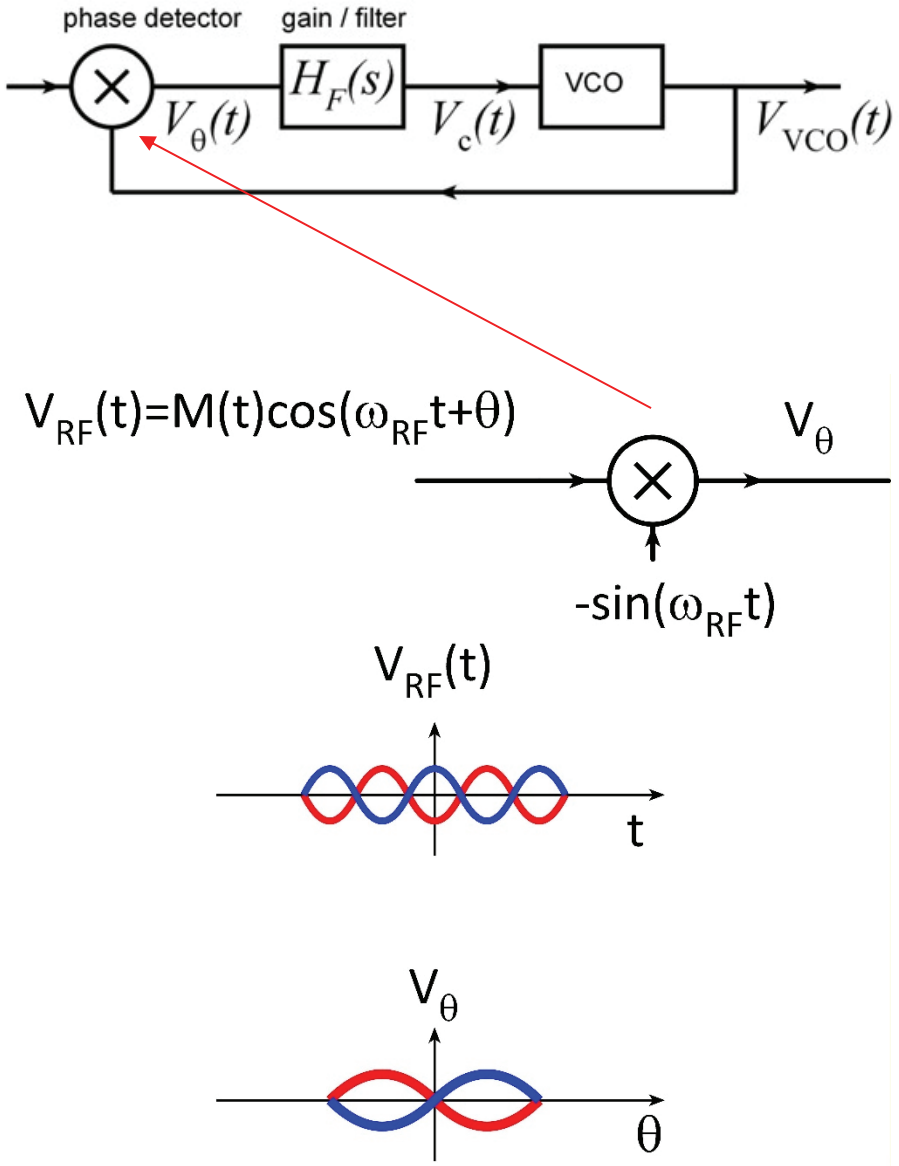
In this figure, the PLL is attempting to lock the VCO to the carrier frequency and phase of received BPSK data

BPSK: $M(t) = +/-1$

$V_\theta \propto M \cdot \sin(\theta)$ changes sign with M.

1/2 the time, the PLL has the wrong sign for its loop transmission.

The loop will not lock on BPSK-modulated data

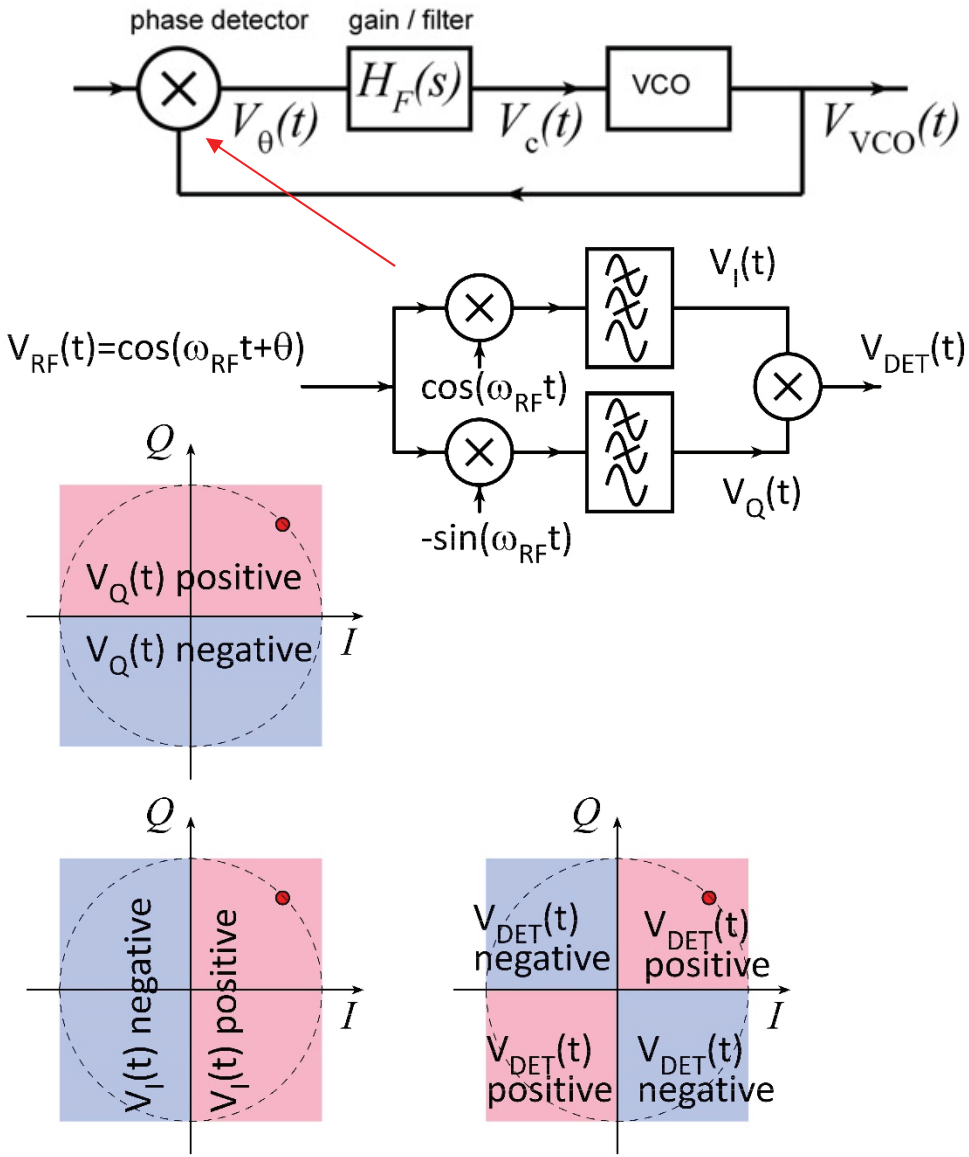


Costas phase detector for BPSK data (1)

Here we use (I,Q) detection, and then take the product

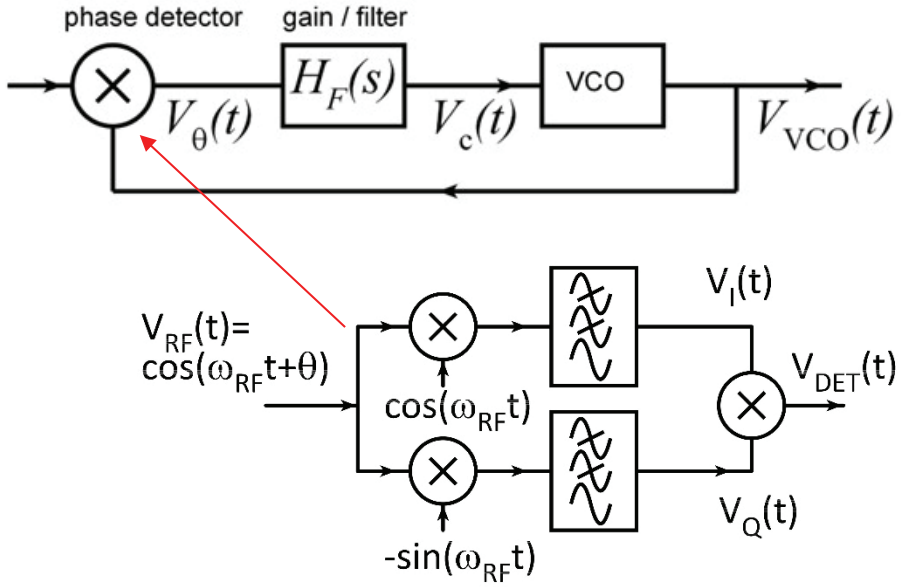
Avoiding math, let us draw pictures instead.

The output, V_{DET} , is positive, in the pink region in the (I,Q) plane.

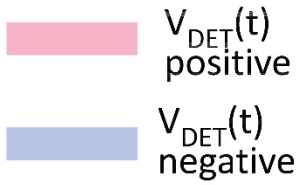


Costas phase detector for BPSK data (2)

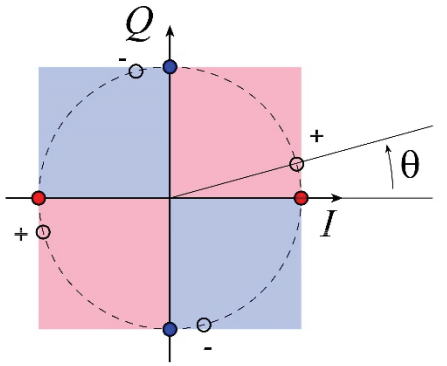
Assume loop is designed such that positive V_θ results in a positive VCO phase (and frequency) shift. This will give the desired negative T_{DC} as long as $dV_\theta / d\theta$ is positive.



At the indicated red points, $dV_\theta / d\theta$ is positive.
.... so T_{DC} is negative.
...these are stable phase-lock points.
...the loop will lock there.



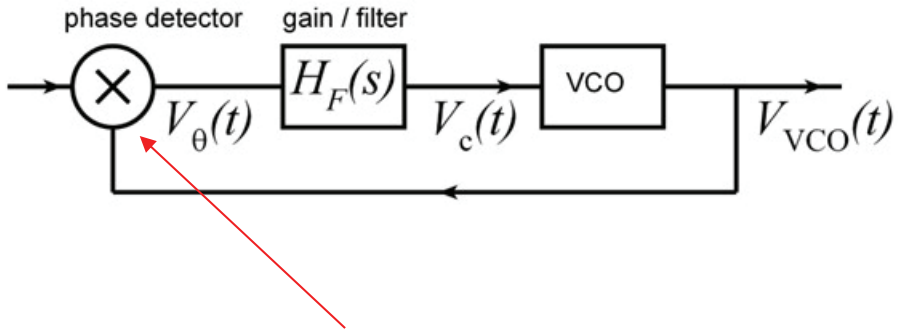
At the indicated blue points, $dV_\theta / d\theta$ is negative.
.... so T_{DC} is positive.
...these are unstable phase points...
the loop will not lock there.

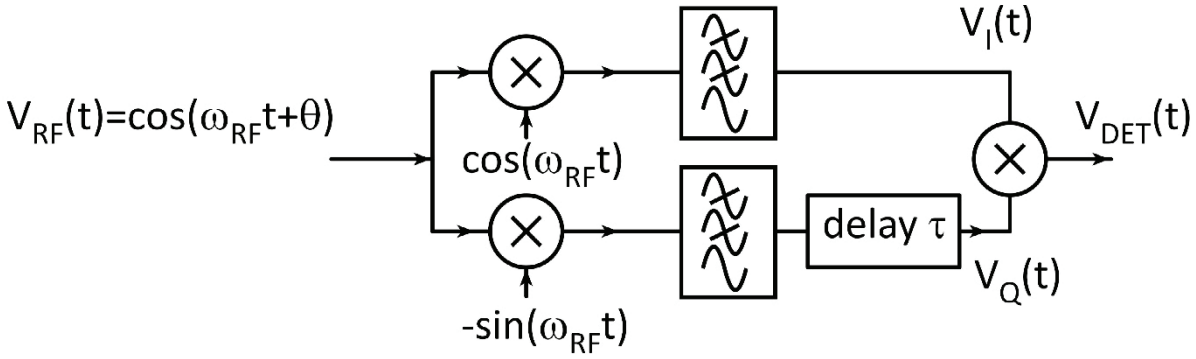


This structure, the Costas phase detector, is used for BPSK carrier recovery PLLs.

Costas phase-frequency detector for BPSK data

Adding the delay τ adds the frequency difference detector.





Extended Costas Detector for QPSK.

We produce the signals

$V_I(t), V_Q(t), V_I(t)+V_Q(t),$ and $V_I(t)-V_Q(t)$

...and then multiply them to form

$$V_{DET} = -1 \cdot V_I(t) \cdot V_Q(t) \cdot \left(V_I(t)+V_Q(t)\right) \cdot \left(V_I(t)-V_Q(t)\right)$$

This produces the +/- pattern shown....

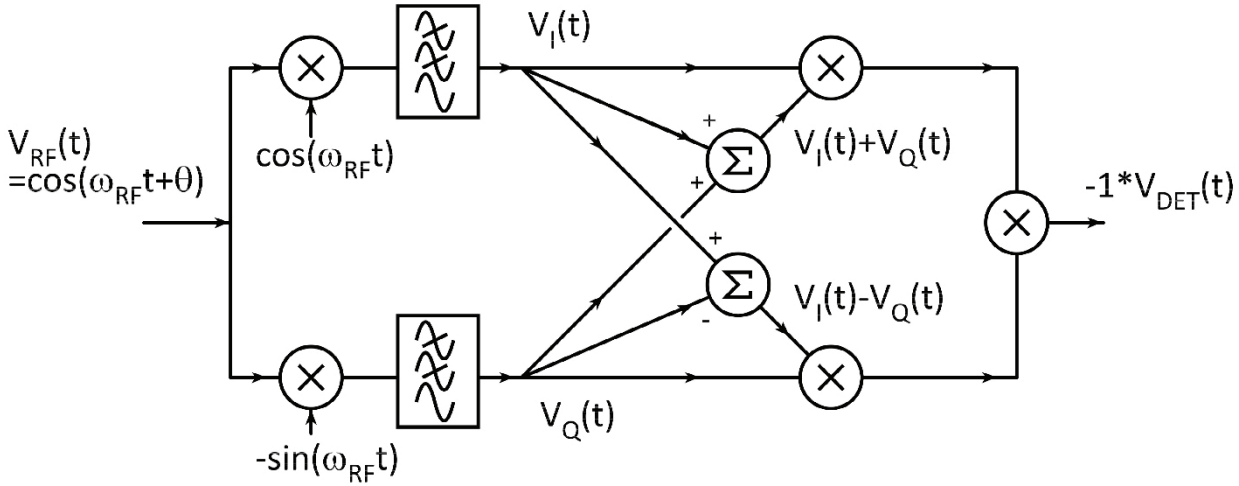
and, with the correct sign of the loop gain,

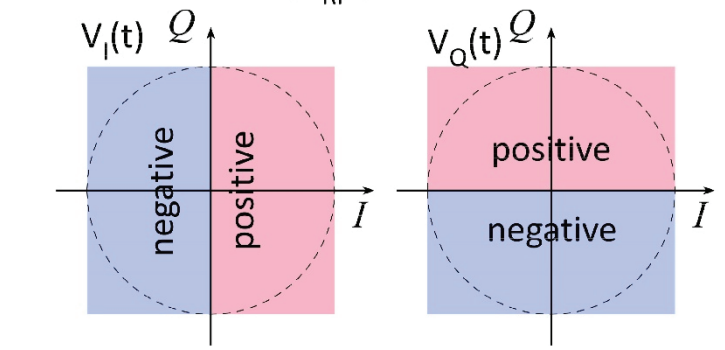
the red points will be stable lock points,

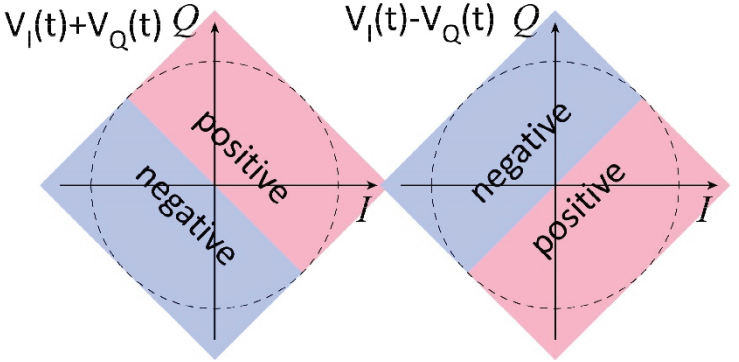
and will work with QPSK modulated signals.

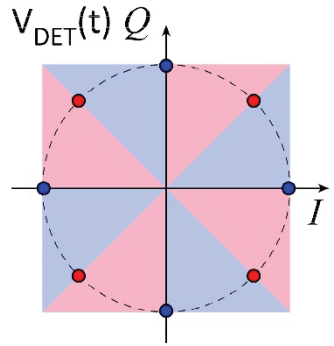
Caution: check for sign errors in my diagram...

Comment: we can add a delay stage to obtain frequency difference detection.









Phase recovery for more complex modulation

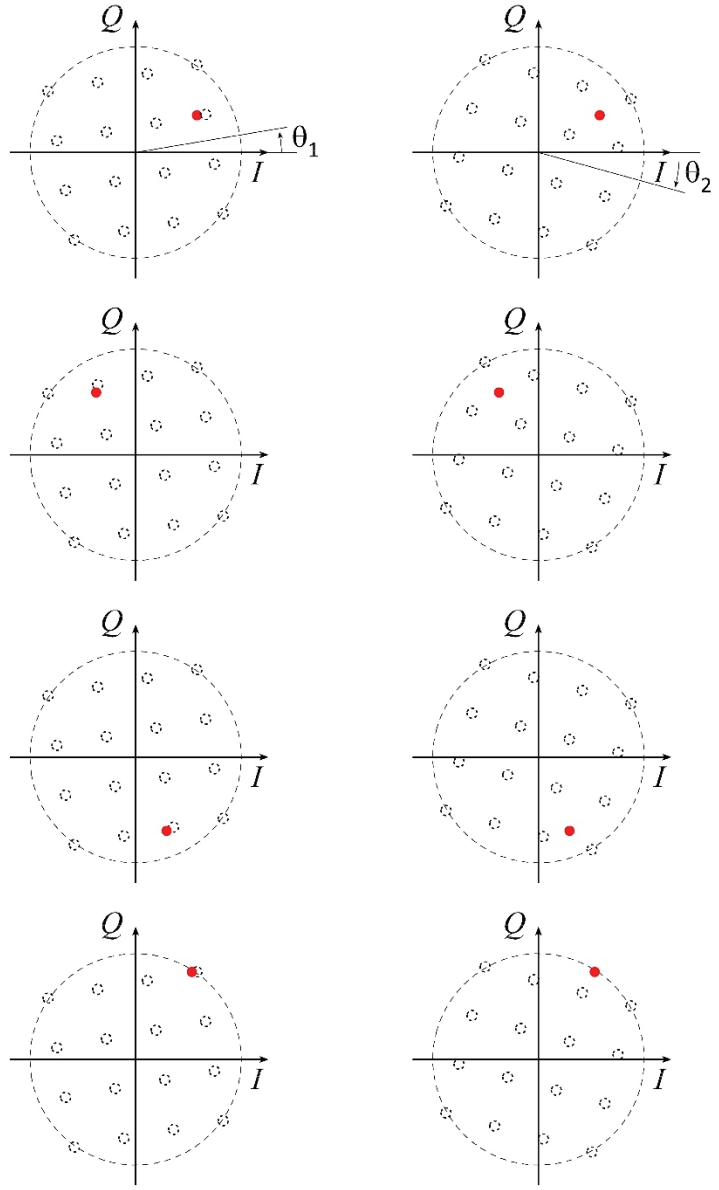
I don't have direct knowledge about how this is done...
....I am guessing.

But, timing recovery for 16,64,...QAM will be too complex for a simple analog circuit implementation.

I suspect this is done with digital signal processing.

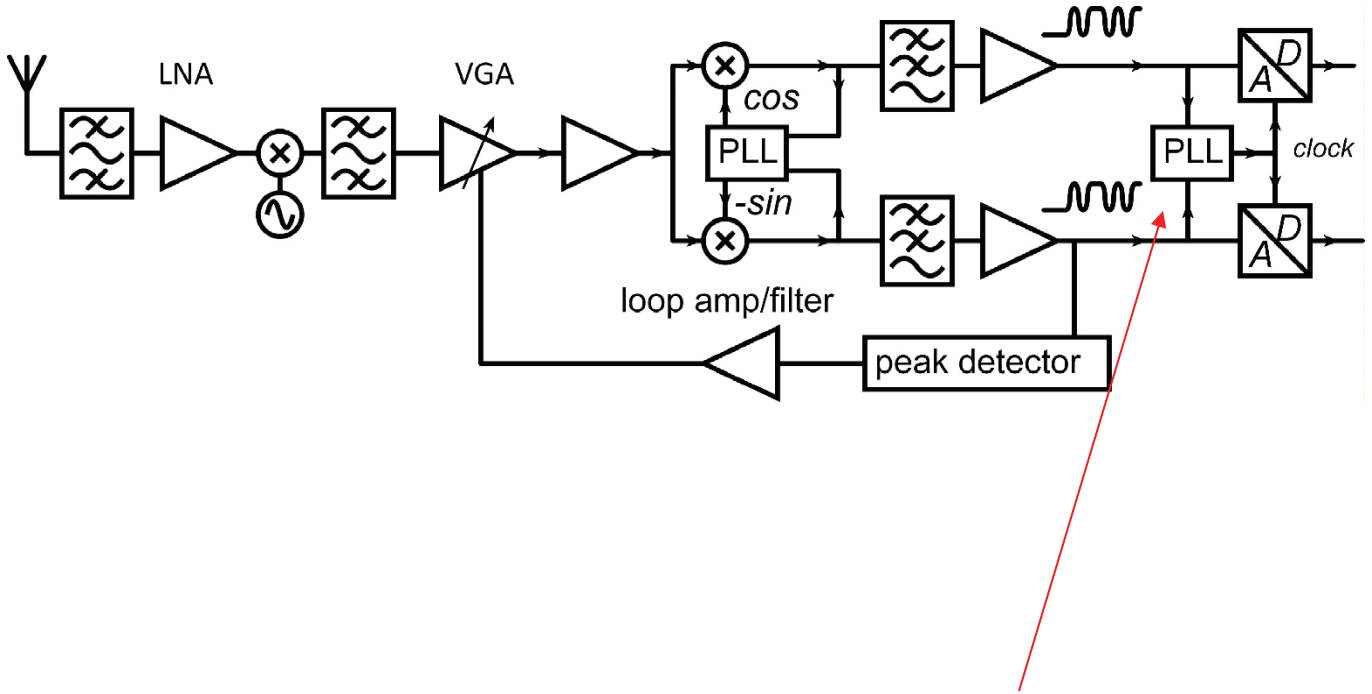
The principle: given a set of observed signals in the (I,Q) plane, for some # of symbol periods, what estimated phase shift $(\theta_1, \theta_2, ...)$ best fits the expected constellation ?

This estimate must consider other impairments (noise, gain errors, etc)



Symbol period recovery (1).

We now must also consider
how to recover
the symbol frequency
and
the symbol timing (phase)



Symbol period recovery (2).

center of symbol periods: $t_1, t_3, t_5, t_7, \ldots$

to recover data, measure the symbol voltages at these times.

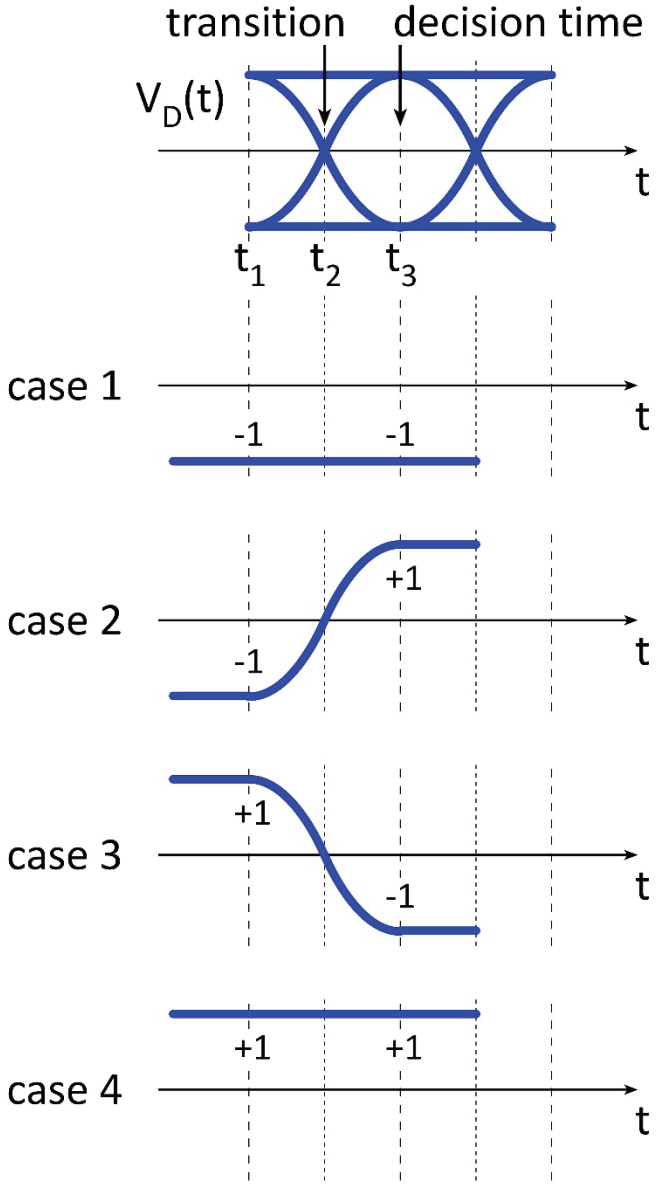
transitions (zero-crossings): $t_2, t_4, t_6, t_8, \ldots$

use these crossings to detect symbol timing.

cases 1 and 4: no transition; can't detect timing

case 2: zero-crossing with positive slope.

case 3: zero-crossing with negative slope.



Symbol period recovery (3).

Transition detection voltage

$V_{DET} = V(t_2) \cdot (V(t_3) - V(t_1))$

cases 1 and 4: $V_{DET} = 0$ (as desired)

case 2: $(V(t_3) - V(t_1)) > 0$

If transition is before sampling time, $V(t_2) > 0$

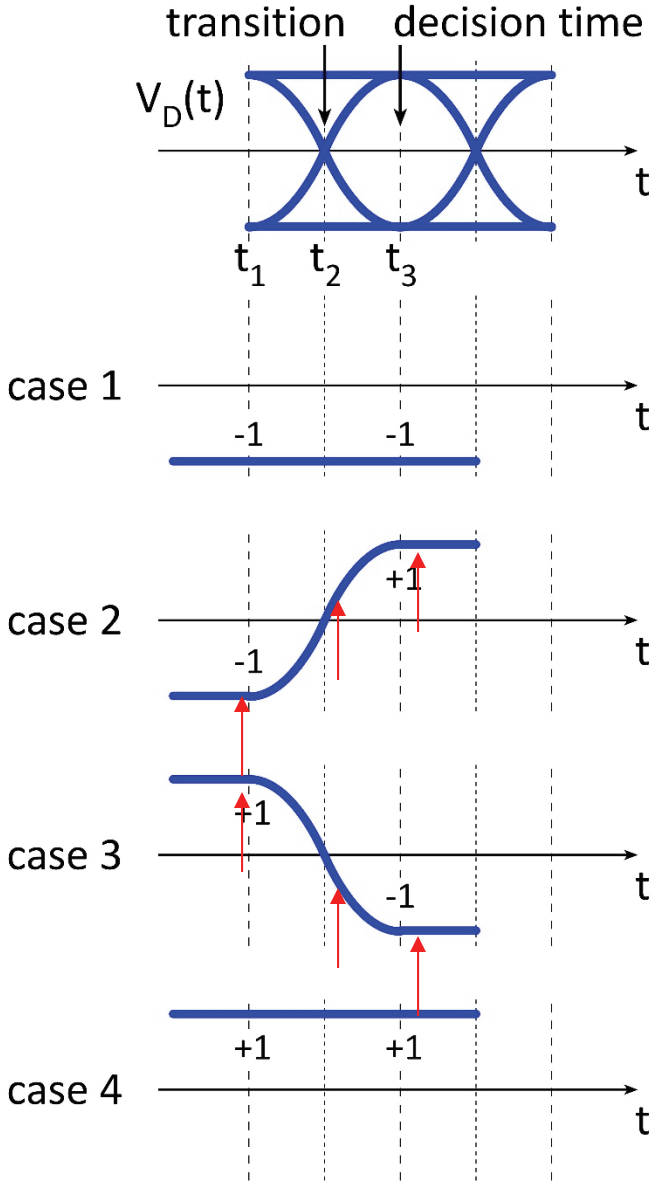
$\rightarrow V_{DET} > 0$

case 3: $(V(t_3) - V(t_1)) < 0$

If transition is before sampling time, $V(t_2) < 0$

$\rightarrow V_{DET} > 0$

Transition before sampling time gives $V_{DET} > 0$



Symbol period recovery (3).

This circuit implements the function

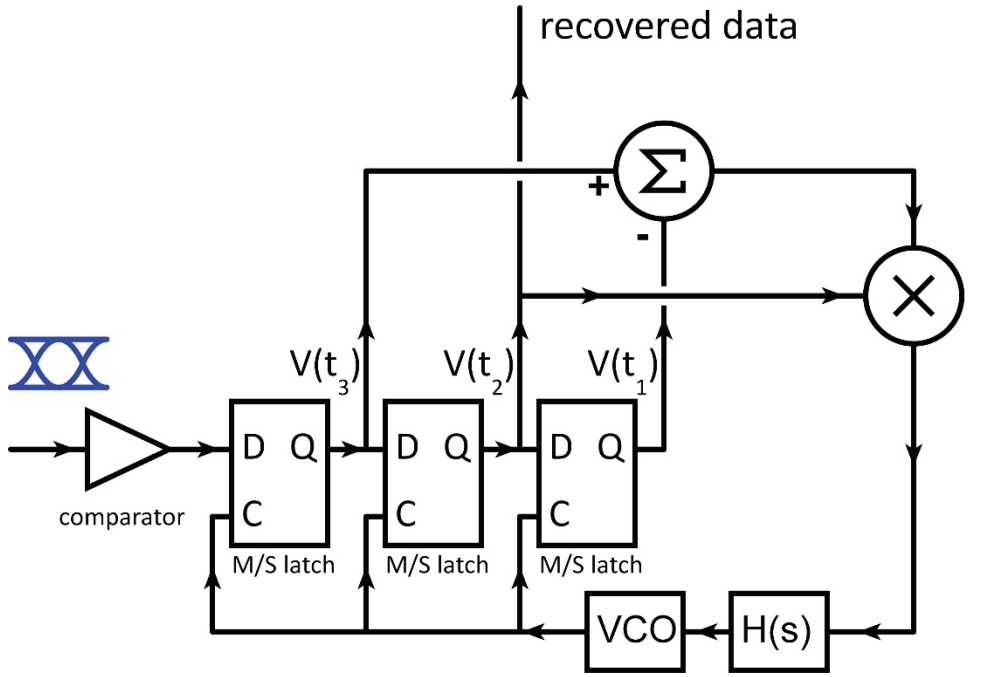
$$V_{DET} = V(t_2) \cdot (V(t_3) - V(t_1))$$

Design is for 2-level signals
I and Q channels of QPSK
2-level signalling in wireline and optical

Some type of frequency difference detector
is also necessary (but not shown)

I am sure this can be generalized to more levels.
See the literature.

At lower symbol rates, DSP techniques
are probably preferred



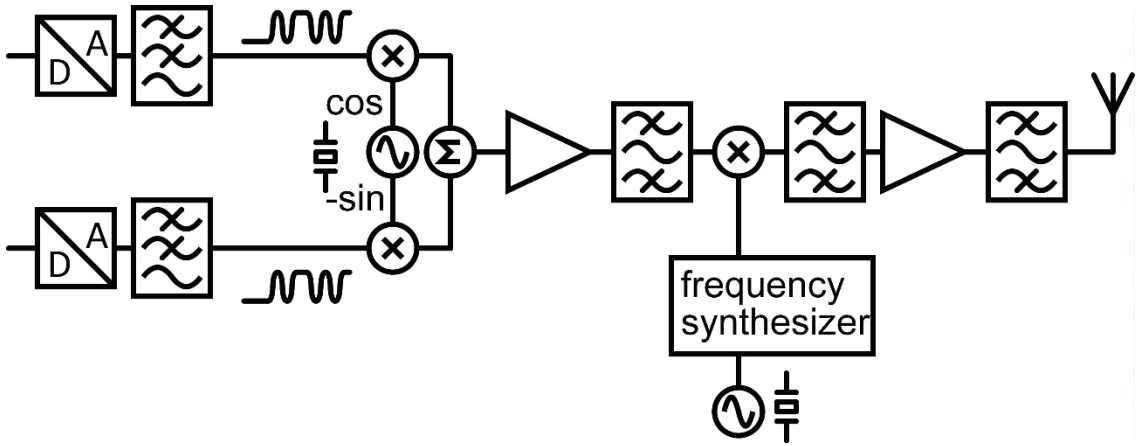
VCO frequency is at *twice* the symbol frequency

Frequency Synthesis

Many transmitters must operate over range of precisely-controlled frequencies.

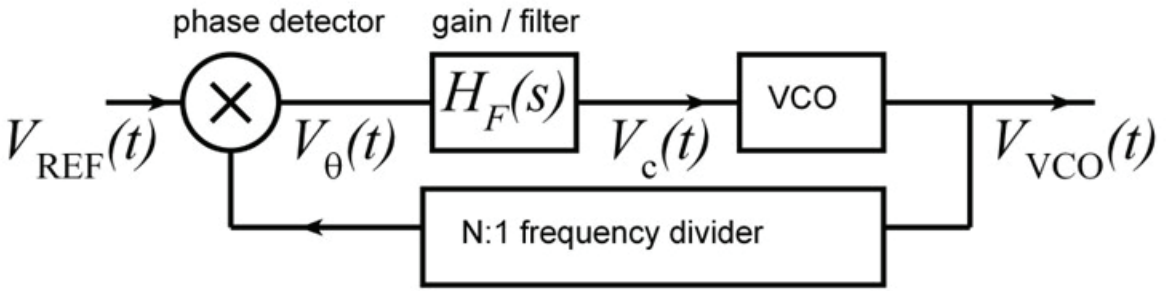
This is called frequency synthesis.

How is it done ?



Frequency Synthesis

Frequency divider:
a digital counter which counts
clock pulses, reaching count N,
and then resetting.



$\rightarrow$ Output frequency is 1/N times the input frequency.
(also: output phase is 1/N times the input phase)

Divider in the feedback path
$\rightarrow$ VCO frequency ω_{VCO} forced to $N\omega_{REF}$

Frequency Synthesis

To tune the VCO frequency, the divider ratio is tuned.

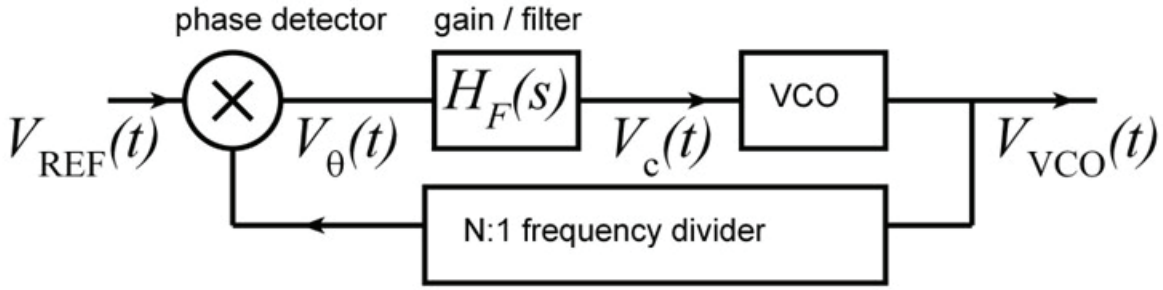
This is done dynamically, by dithering the divider ratio between N and $(N+1)$.

The dithering is done at a rate much larger than the loop bandwidth.

Dithering techniques:

delta sigma

fractional frequency synthesis



Delta Sigma Frequency Synthesis (1)

Analyze a simple *first-order* delta sigma DAC

Truncator takes M-bit word, and simply ignores all but most significant bit.

Truncator input: $N_2(t)$

Truncator output: $N_{out}(t) = N_2(t) - \varepsilon$

ε : rounding error associated with truncation.

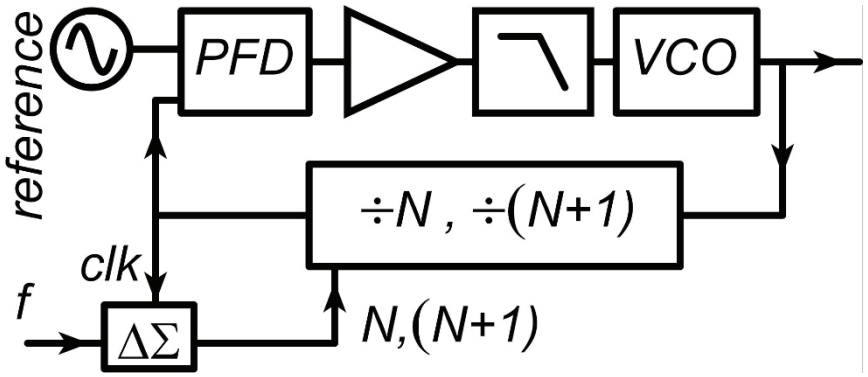
model as white noise (but not Gaussian)

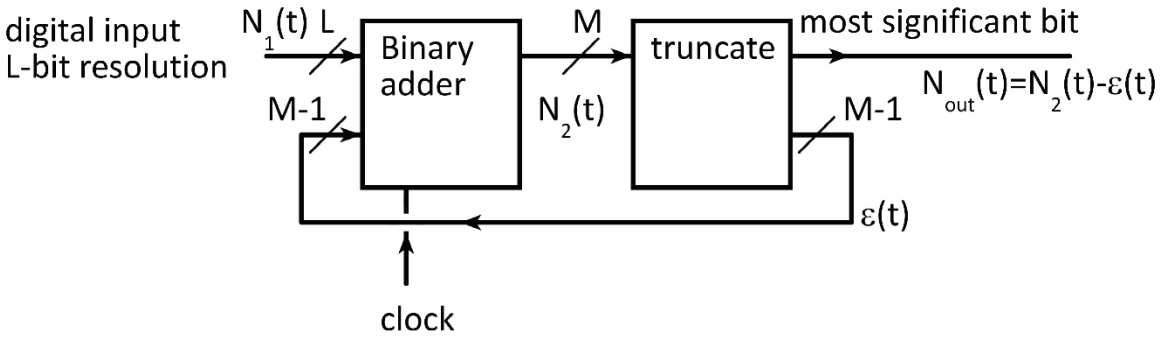
$$N_2(t - t_{clock}) = N_1(t) + \varepsilon(t)$$

$$N_2 \exp(-j\omega t_{clock}) = N_1 + \varepsilon$$

$$N_2 = \frac{N_1 + \varepsilon}{\exp(-j\omega t_{clock})}$$

$$N_{out} = N_2 - \varepsilon = \frac{N_1 + \varepsilon}{\exp(-j\omega t_{clock})} - \frac{\varepsilon \exp(-j\omega t_{clock})}{\exp(-j\omega t_{clock})}$$





Please see M. H. Perrott, M. D. Trott and C. G. Sodini, "A modeling approach for /spl Sigma/-/spl Delta/ fractional-N frequency synthesizers allowing straightforward noise analysis," in *IEEE Journal of Solid-State Circuits*, vol. 37, no. 8, pp. 1028-1038, Aug. 2002, doi: 10.1109/JSSC.2002.800925.

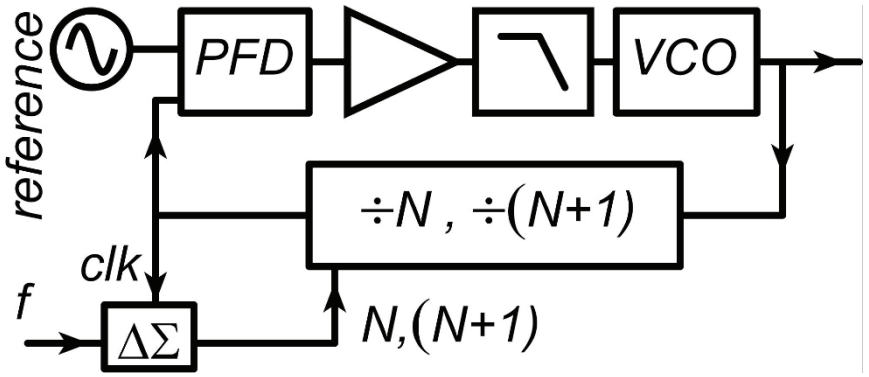
Delta Sigma Frequency Synthesis (2)

$$N_{out} = \frac{N_1 + \varepsilon(1-\exp(-j\omega t_{clock}))}{\exp(-j\omega t_{clock})}$$

$$\xrightarrow{\omega t_{clock} << 1} \frac{N_1 + j\omega t_{clock}\varepsilon}{1 - j\omega t_{clock}} \cong N_1 + j\omega t_{clock}\varepsilon$$

$$N_{out}(j\omega) = N_1 + H_N(j\omega)\varepsilon(j\omega)$$

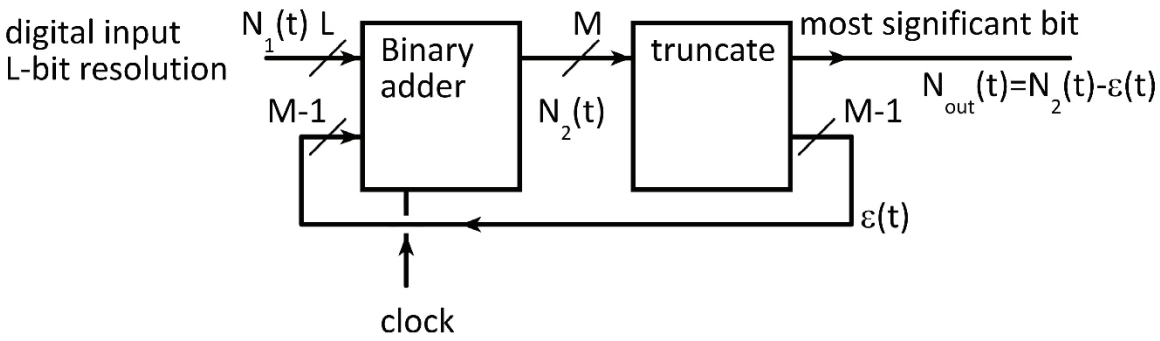
where $H_N(j\omega) \cong j\omega t_{clock}$ is the *noise transfer function*



Spectral density of truncation error:

$$S_{N_{out}}(j\omega) = \| H_N(j\omega) \|^2 \; S_\varepsilon(j\omega) = \omega^2 t_{clock}^2 S_\varepsilon(j\omega)$$

key point: $\| H_N(j\omega) \|^2 <<<< 1$ for $(\omega t_{clock}) << 1$



If well-designed, quantization noise of the delta-sigma modulator will be at high frequencies, outside PLL bandwidth

Please see M. H. Perrott, M. D. Trott and C. G. Sodini, "A modeling approach for /spl Sigma/-/spl Delta/ fractional-N frequency synthesizers allowing straightforward noise analysis," in *IEEE Journal of Solid-State Circuits*, vol. 37, no. 8, pp. 1028-1038, Aug. 2002, doi: 10.1109/JSSC.2002.800925.

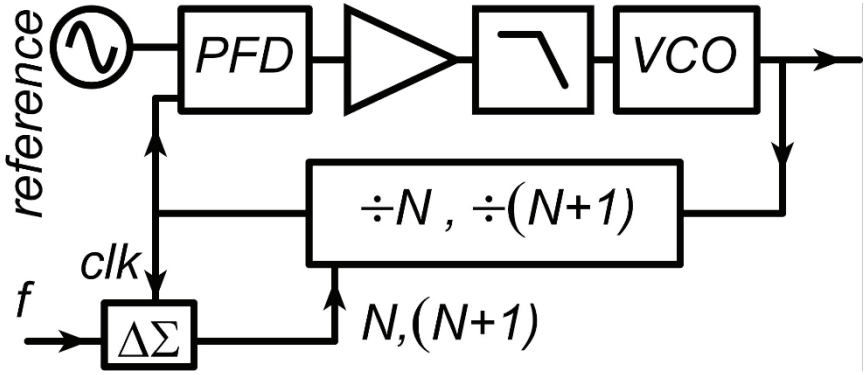
Delta Sigma Frequency Synthesis (3)

The prior analysis was for a first-order delta-sigma DAC

which gave :

$$S_{N_{out}}(j\omega) = \| H_N(j\omega) \|^2 \; S_\varepsilon(j\omega)$$

where $\| H_N(j\omega) \|^2 \approx \omega^2 t_{clock}^2$



Typical delta-sigma PLLs use **second order** DACs, which give

$$\| H_N(j\omega) \|^2 \approx \omega^4 t_{clock}^4$$

Quantization noise within PLL bandwidth is even

better suppressed.

Please see M. H. Perrott, M. D. Trott and C. G. Sodini, "A modeling approach for /spl Sigma/-/spl Delta/ fractional-N frequency synthesizers allowing straightforward noise analysis," in *IEEE Journal of Solid-State Circuits*, vol. 37, no. 8, pp. 1028-1038, Aug. 2002, doi: 10.1109/JSSC.2002.800925.

Loop Phase Transfer Function.

Loop Transmission:

$$T(s) = \frac{K_{pd} K_{VCO} (1 + s\tau_z)}{N s^2 \tau_i}$$

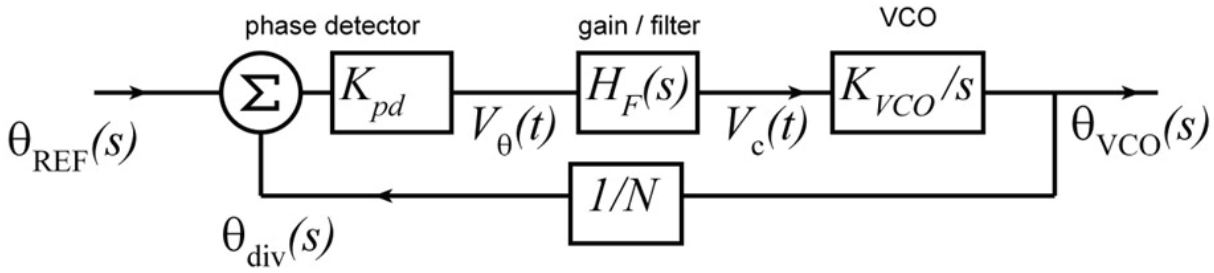
If the loop filter is $H_F(s) = (1 + s\tau_z) / s\tau_i$, then

$$T(s) = \frac{K_{pd} K_{VCO} (1 + s\tau_z)}{N s^2 \tau_i} = \frac{\omega_x^2 (1 + s/\omega_z)}{s^2}; \quad \text{where } \omega_x^2 = \frac{K_{pd} K_{VCO}}{N \tau_i}$$

Phase transfer function:

$$\frac{\theta_{VCO}(s)}{\theta_{REF}(s)} = N \frac{T(s)}{1 + T(s)}$$

Note the N:1 increase in phase deviation.



Phase Noise Transfer Functions

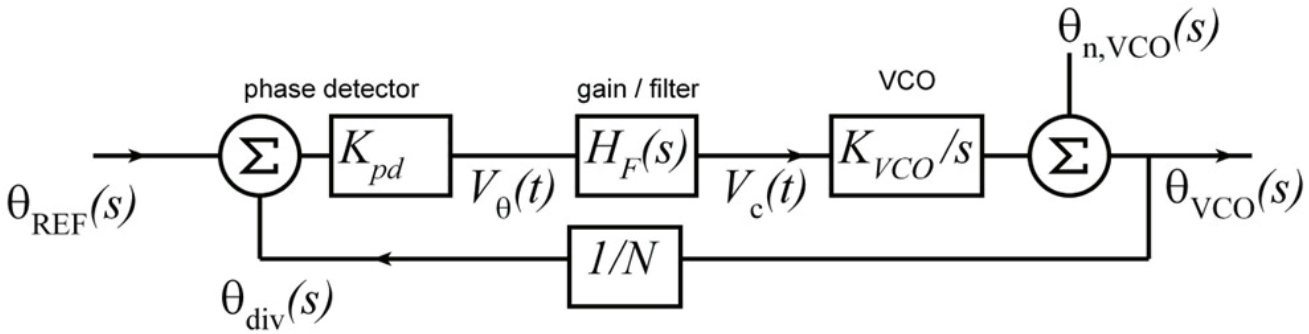
$\theta_{N,VCO}$ is the (outcome of) the VCO phase noise.

$$\theta_{VCO} = \theta_{N,VCO} + \frac{K_{pd}K_{VCO}H_f(s)}{s}\left(\theta_{REF} - \theta_{VCO}/N\right)$$

$$= \theta_{N,VCO} + \frac{K_{pd}K_{VCO}H_f(s)}{Ns}\left(N\theta_{REF} - \theta_{VCO}\right)$$

$$\theta_{VCO} = \theta_{N,VCO} + T(s)\left(N\theta_{REF} - \theta_{VCO}\right)$$

$$\theta_{VCO} = \frac{1}{1+T(s)}\theta_{N,VCO} + \frac{T(s)}{1+T(s)}(N\theta_{REF})$$



The closed-loop phase deviations θ_{VCO} include
the open loop VCO phase deviations $\theta_{N,VCO}$ multiplied by 1/(1+T)
and the reference phase deviations multiplied by T/(1+T)

If delta-sigma synthesis is used, there are additional noise terms