ECE 145C / 218C, notes set xx: Class A Power Amplifiers

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Class A power amplifier

Class A: amplifier that is at least nominally linear for small to moderate-amplitude input signals.

Clearly clips (limits) for large output voltages.

Maximum voltage $V_{\max}$

Minimum voltage $V_{\min}$

Maximum current $I_{\max}$

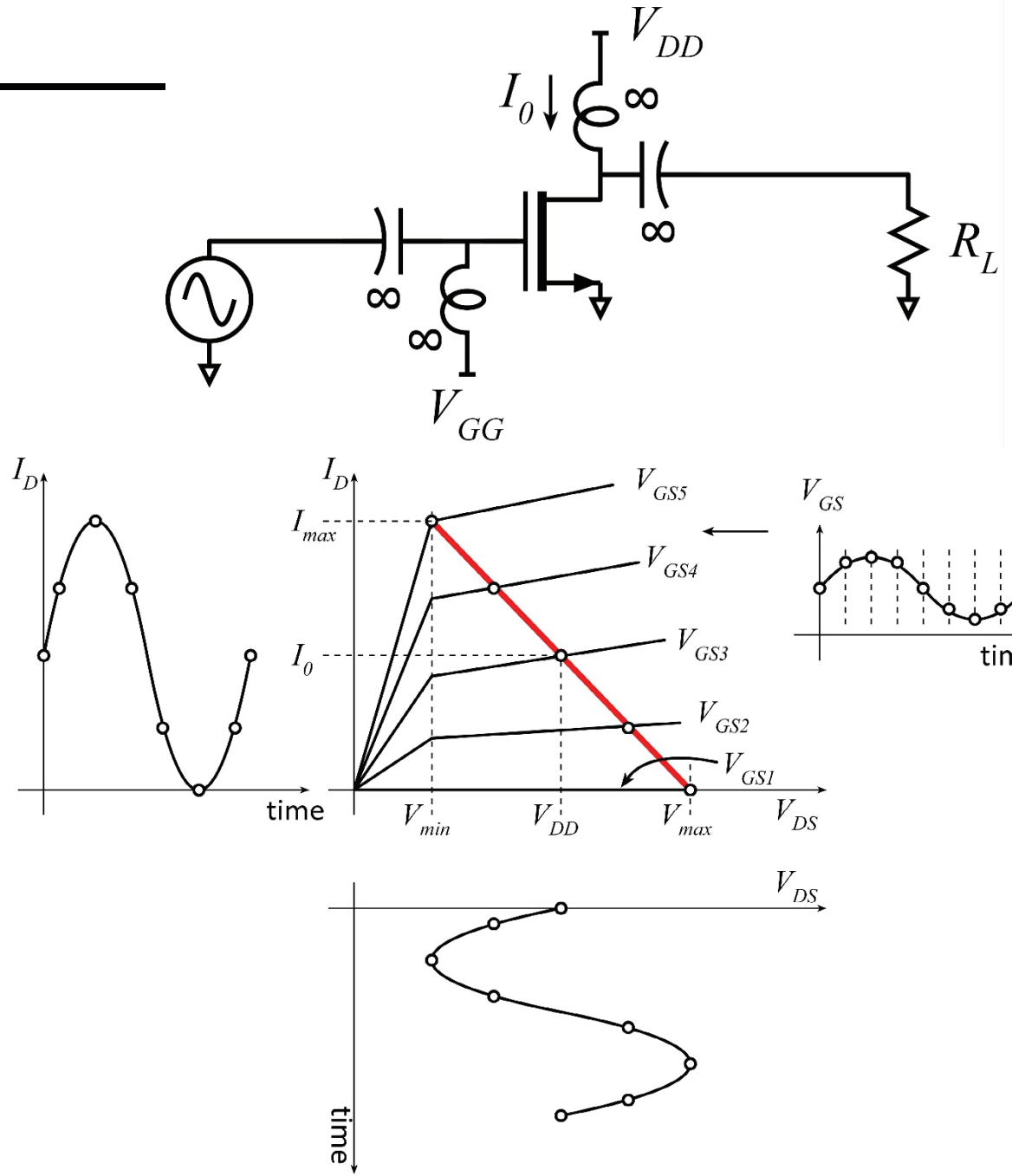
Bias drain current I_0

Bias drain voltage V_{DD}

If FET $I-V$ characteristics were linear then

$I_0 = I_{\max}/2;\ V_{DD} = (V_{\max} - V_{\min})/2.$

....but real transistors are not perfectly linear



Transistor Output Characteristics

Idealized:

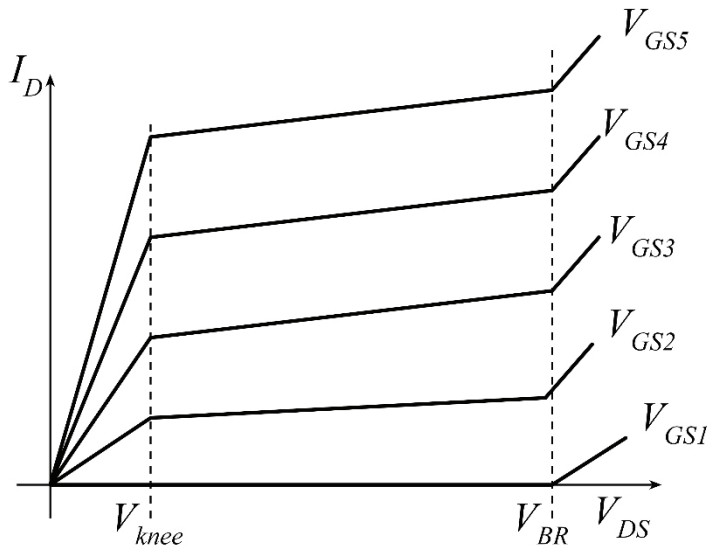
Minimum voltage: V_{knee}

Maximum voltage: V_{br}

Maximum current: $I_{\max}$

FETs: $I_{\max} \propto$ (gate width)(# gate fingers) $= N_g W_g$,

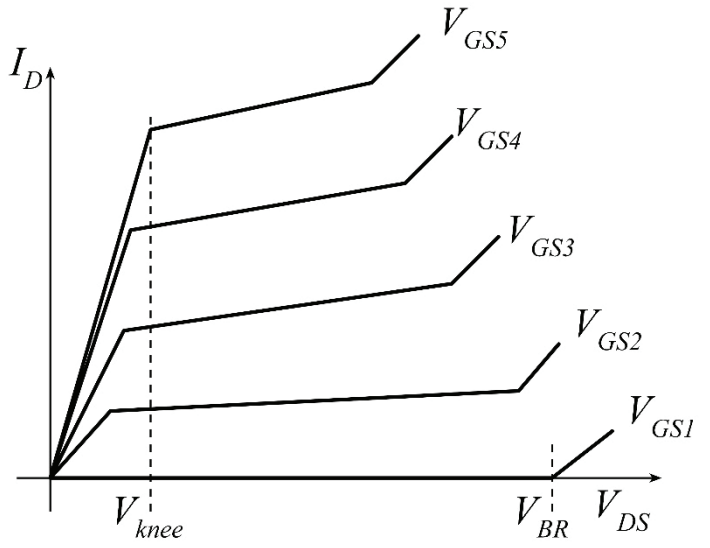
bipolars: $I_{\max} \propto$ (emitter length)(# emitter fingers) $= N_e L_e$



Real

V_{br} depends on I_D or I_C

V_{knee} depends on I_D or I_C



Comments/Caution

Textbooks: $V_{knee} = V_{sat}$; Reality V_{knee} due to many factors

Textbooks: bipolar $V_{BR} = V_{BRCBO}, V_{BRCEO}$ etc. ; Reality is much more complicated.

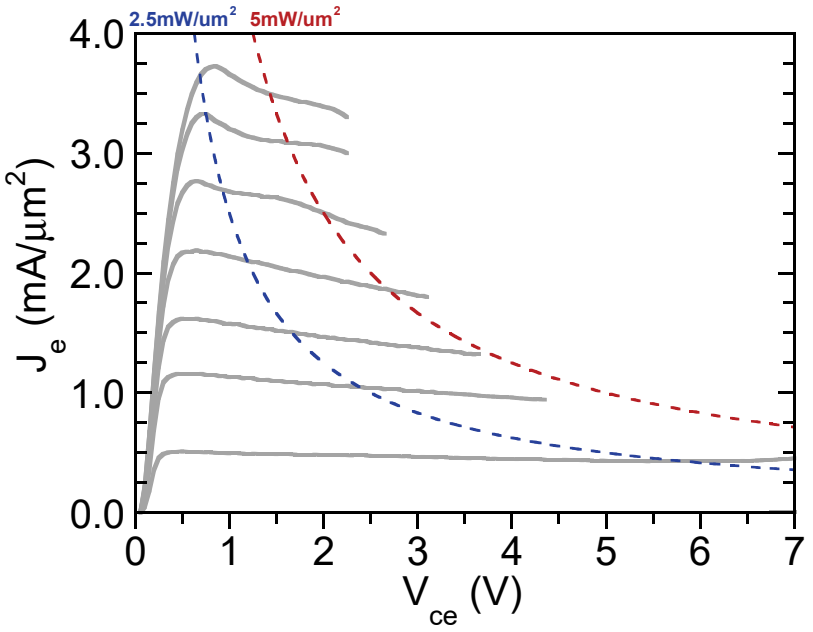
Transistor Output Characteristics: measured

250nm InP HBT

I_E = (emitter current density)(total emitter area)

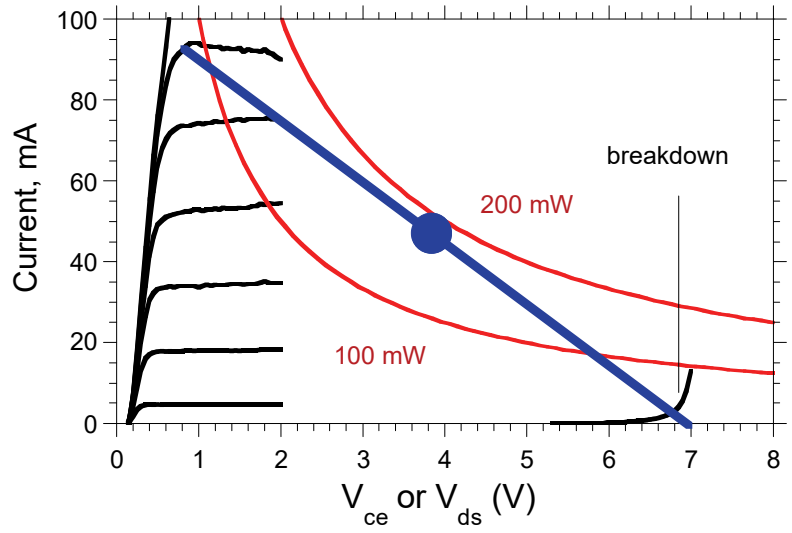
$= J_E$(number emitter fingers)(emitter area per finger)

$= J_E N_E A_E$



500nm InP HBT

(not sure what emitter area this is)



For I-V curves of state-of-art MOSFETs,

please see recent IEDM conference digests.

Transistor Output Characteristics: Instantaneous Power Contours

Instantaneous dissipated power $= V_{ce} I_c$ or $V_{DS} I_D$

Constant power contours: hyperbolas on I_{out}, V_{out} plane

Low-frequency power amplifier

signal frequency $<<$ (thermal time constant)$^{-1} = \tau_{\text{thermal}}^{-1}$

$\rightarrow$ loadline must lie below maximum power density curve

τ_{thermal} can be of order of μs to ns, depending on transistor size.

High-frequency power amplifier

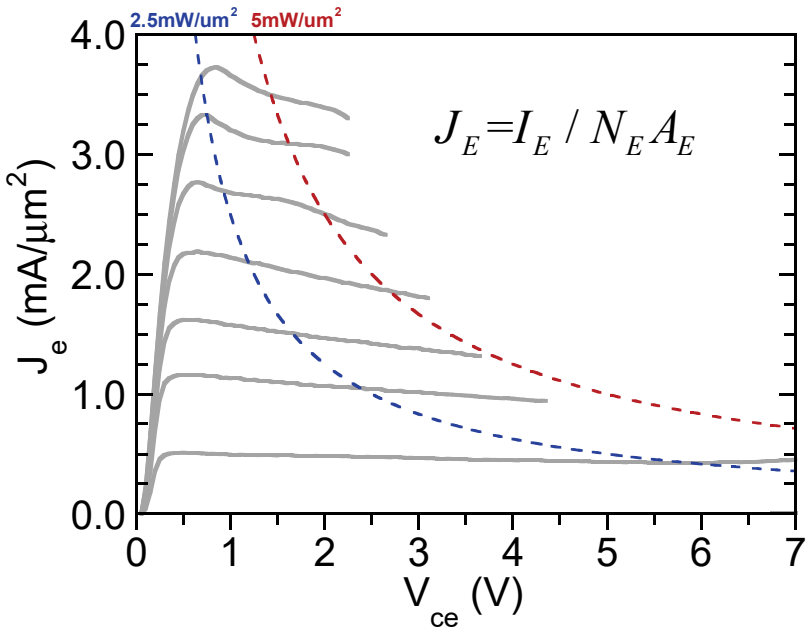
signal frequency $>>$ (thermal time constant)$^{-1}$

$\rightarrow$ *bias point* must lie below maximum power density curve

Note: measured DC (I,V) characteristics are influenced by heating.

Breakdown with $f_{signal} >> \tau_{\text{thermal}}^{-1}$ can be larger than V_{BR} @DC.

RF loadline can surpass DC breakdown voltage.



Transistor parameters and cutoff frequencies vary across (I,V) plane

Bipolar Transistors:

Low voltage and high current:

"Kirk effect" = space-charge-limited current

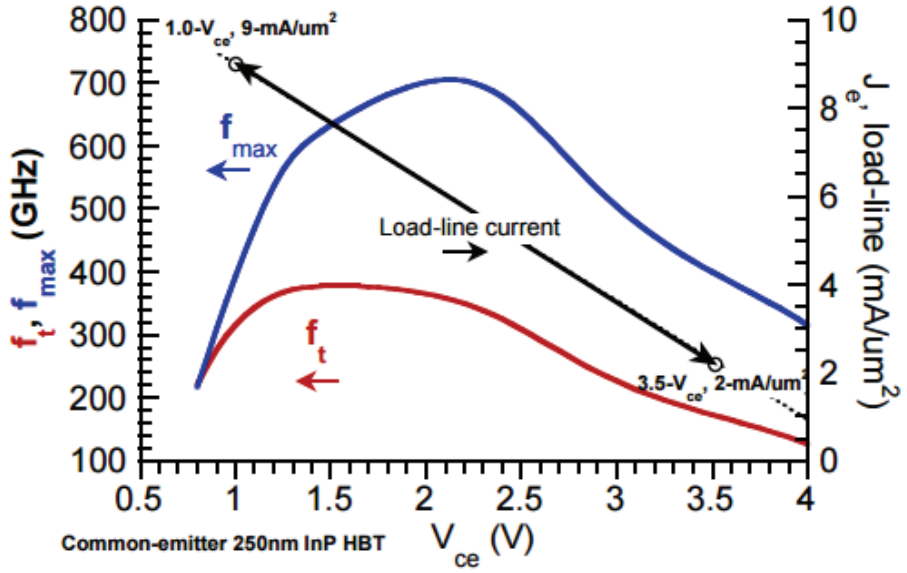
reduction in f_τ, increase in $C_{cb} \rightarrow$ reduced bandwidth

High voltage:

all semiconductors: push-out of collector depletion edge

III-V semiconductors: reduction of electron velocity in collectror

reduction in $f_\tau \rightarrow$ reduced bandwidth



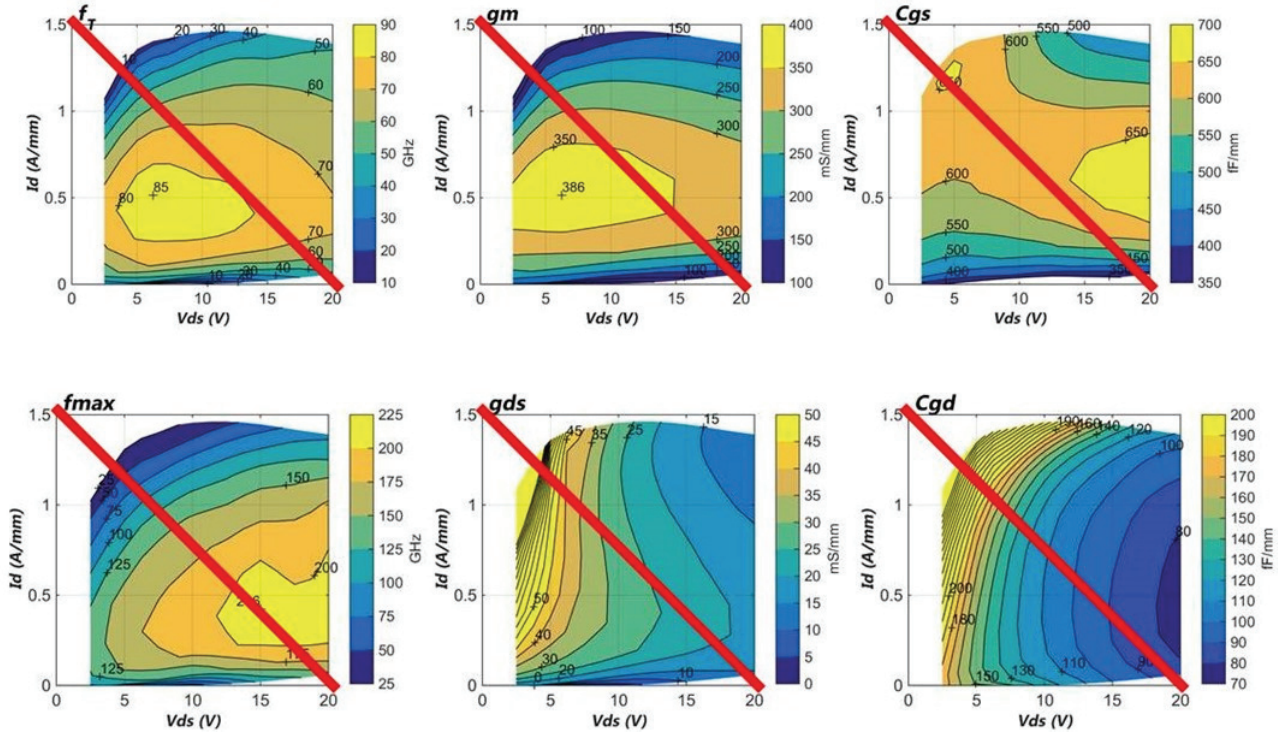
Z. Griffith, 2012 IPRM

Transistor parameters and cutoff frequencies vary across (I,V) plane

Field-Effect Transistors:

Device parameters vary strongly across (I,V) plane

$(f_\tau, f_{\max})$ vary strongly across (I,V) plane



GaN HEMT experimental data (c.a. 2010) due to Kiesuke Shinohara, Teledyne Scientific

Safe Operating Area (SOA); "Fast Operating Area " (FOA ?)

Safe operating area

standard terminology

region bounded by maximum power hyperbola, V_{br}, $I_{\max}$

SOA includes other effects beyond the scope of these notes

"Fast operating area"

not standard terminology

region with adequately high $f_t, f_{\max}$

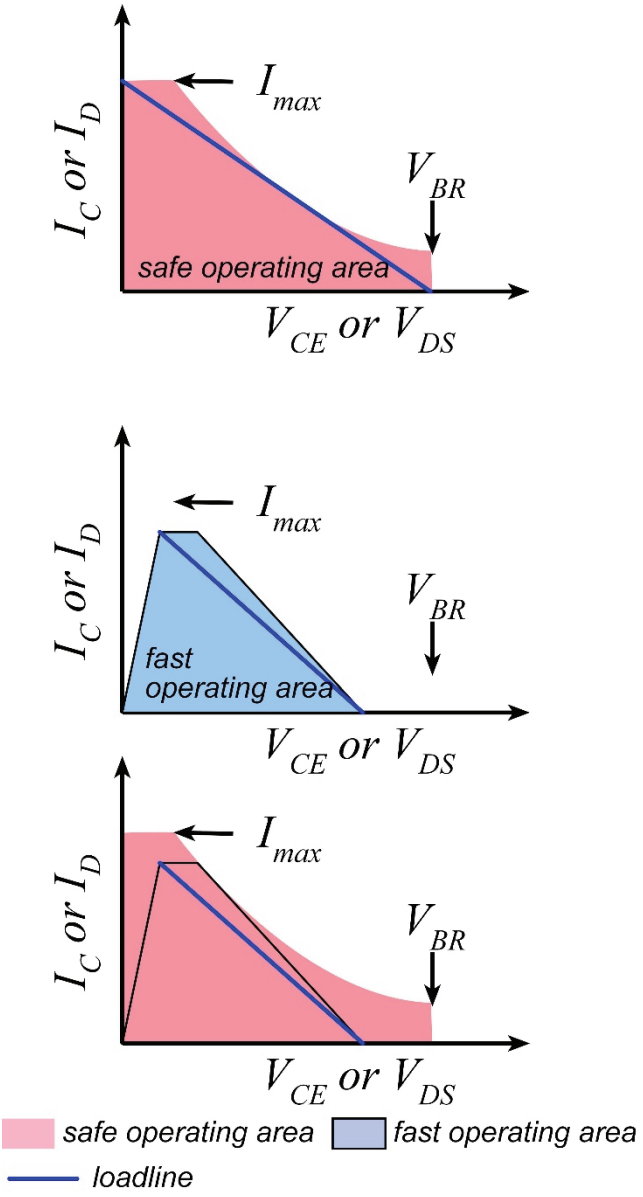
Loadline must lie within both

Reliability

Particularly with Si MOSFETs,

reliability deceases as V_{DS} increases.

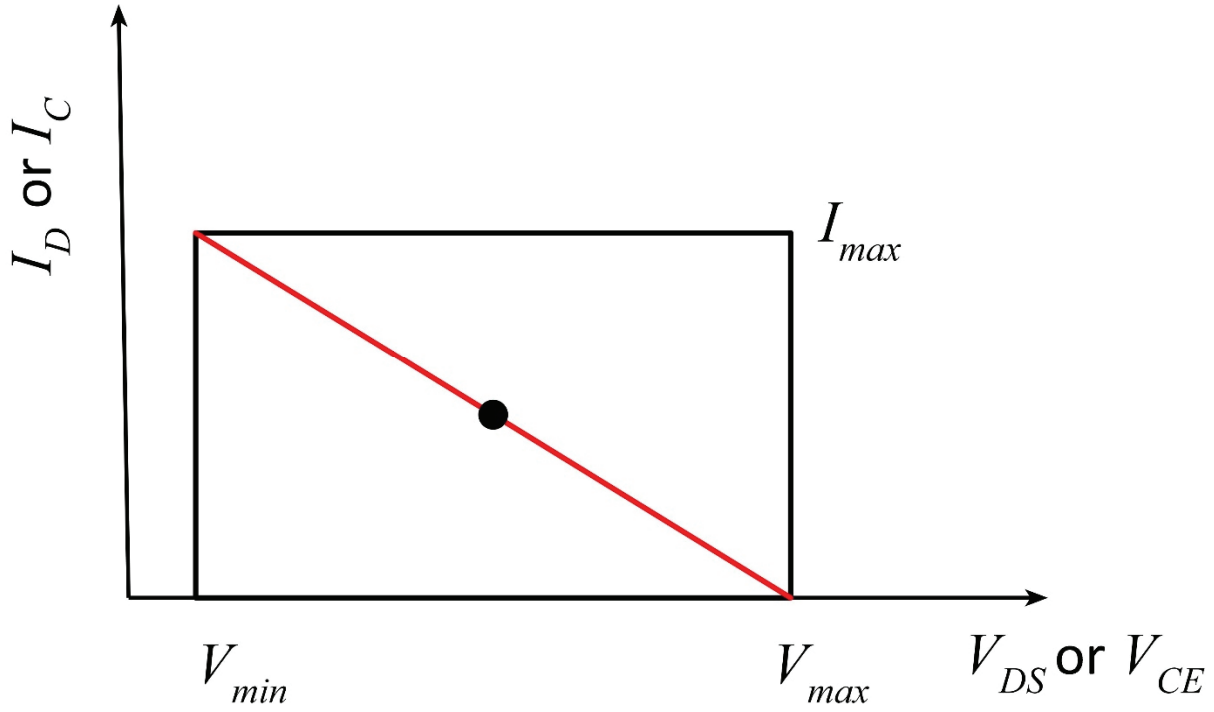
$\rightarrow$ maximum V_{DS} well below DC breakdown



Oversimplified SOA/FOA; for class

Maximum, minimum voltages

Maximum current $\propto$ $N_g W_g$ or $N_E L_E$



Simple class A power analysis

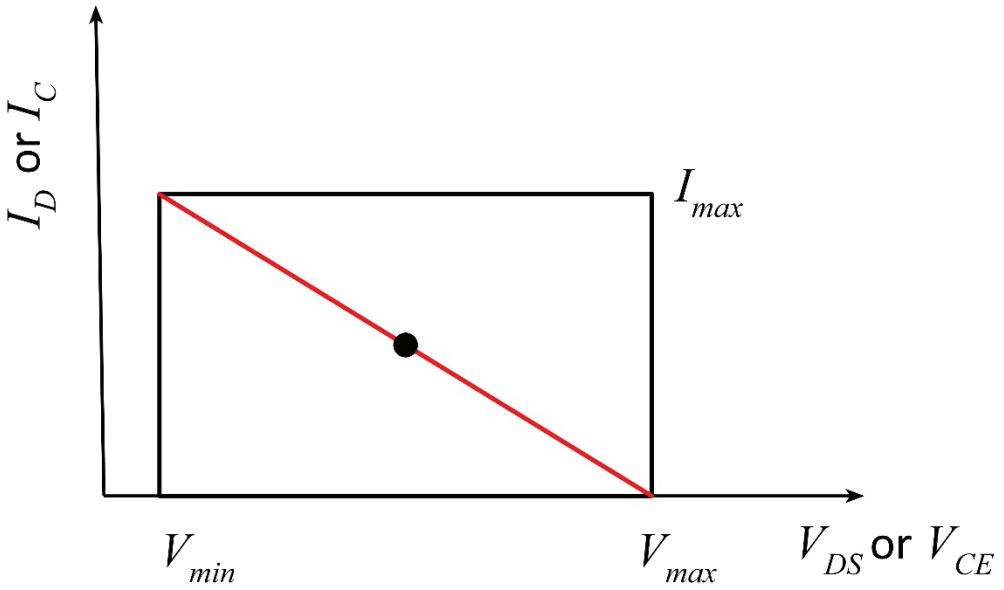
Bias point in center of rectangle.

Loadline reaches corners of rectangle

$$Z_L = R_L + j0\Omega = (V_{\max} - V_{\min}) / I_{\max}$$

$$P_{DC} = V_{DC} I_{DC} = (V_{\max} + V_{\min}) I_{\max} / 4$$

$$P_{RF,\max} = (V_{\max} - V_{\min}) I_{\max} / 8 = (V_{\max} - V_{\min})^2 / 8R_L$$



drain/collector efficiency at peak output power

$$\eta_{\text{drain/collector}} = \frac{P_{RF,\max}}{P_{DC}} = \frac{(V_{\max} - V_{\min}) I_{\max} / 8}{(V_{\max} + V_{\min}) I_{\max} / 4}$$

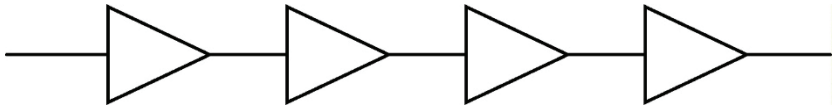
$$\eta_{\text{drain/collector}} = \frac{1}{2} \frac{V_{\max} - V_{\min}}{V_{\max} + V_{\min}}$$

...all expressions correct if and only if $Z_L = (V_{\max} - V_{\min}) / I_{\max}$.

Power-added efficiency

$$\text{P.A.E.} \equiv (P_{out} - P_{in}) / P_{DC}$$

$$= \frac{P_{out}}{P_{DC}}\left[1 - \frac{P_{in}}{P_{out}}\right] = \eta_{\text{drain/collector}} \cdot \left[1 - \frac{1}{\text{gain}}\right] \quad \text{where} \quad \eta_{\text{drain/collector}} = \frac{P_{out}}{P_{DC}}$$



$$\text{PAE}_{overall} = \frac{P_{out,N} - P_{in1}}{P_{DC1} + P_{DC2} + \ldots + P_{DC,N}} = \frac{(P_{out,N} - P_{in,N}) + (P_{out,N-1} - P_{in,N-1}) + \ldots + (P_{out1} - P_{in1})}{P_{DC1} + P_{DC2} + \ldots + P_{DC,N}}$$

$$= \frac{1}{P_{DC1} + P_{DC2} + \ldots + P_{DC,N}}\left(P_{DC,1}\frac{(P_{out,1} - P_{in,1})}{P_{DC,1}} + P_{DC,2}\frac{(P_{out,2} - P_{in,2})}{P_{DC2}} \ldots + P_{DC,N}\frac{(P_{out,N} - P_{in,N})}{P_{DC,N}} \right)$$

$$= \frac{1}{P_{DC1} + P_{DC2} + \ldots + P_{DC,N}}\left(P_{DC,1}\text{PAE}_1 + P_{DC,2}\text{PAE}_2 + \ldots + P_{DC,N}\text{PAE}_N \right)$$

Now suppose $\text{PAE}_1 = \text{PAE}_2 = \ldots = \text{PAE}_N$

$$\text{PAE}_{overall} = \frac{\text{PAE}_1}{P_{DC1} + P_{DC2} + \ldots + P_{DC,N}}\left(P_{DC,1} + P_{DC,2} + \ldots + P_{DC,N} \right) = \text{PAE}_1$$

A PA chain obtains the same overall PAE as that of 1 stage if

each PA has the same PAE and if each stage in the chain reaches that PAE under the same overall RF drive.

Due to accumulated gain compression, real multistage power amplifiers are rarely designed to meet this criterion.

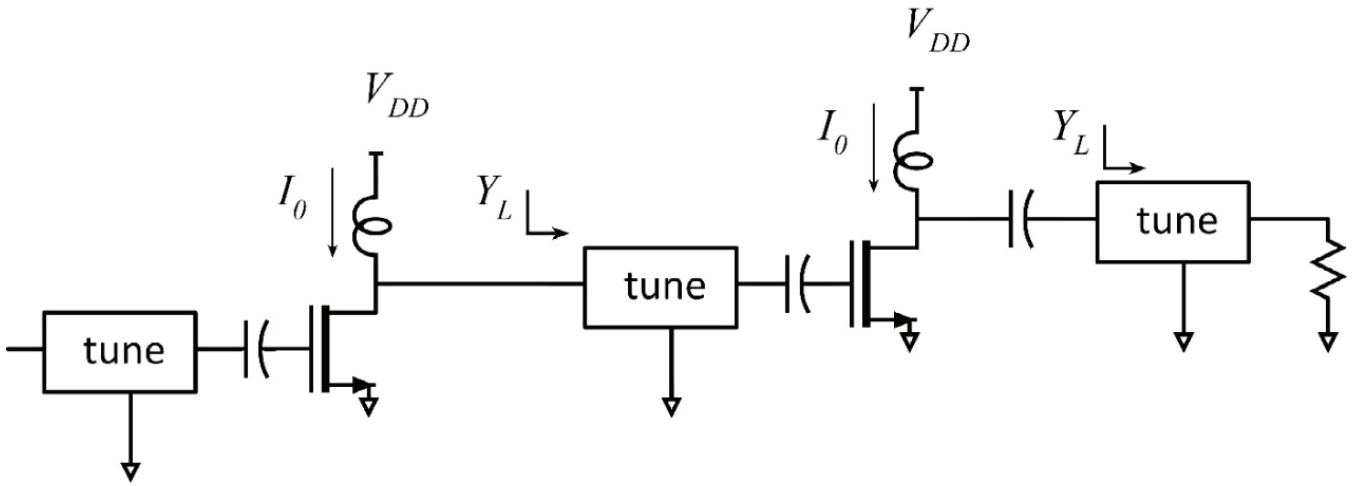
Power Amplifier Design

For highest efficiency, each stage should be loaded with

$$Z_{L,opt} = (V_{\max} - V_{\min}) / I_{\max}$$

The interstage networks are tuning networks,
not matching networks.

Thus far, we have neglected transistor parasitics.



Loadline: inclusive of transistor parasitics

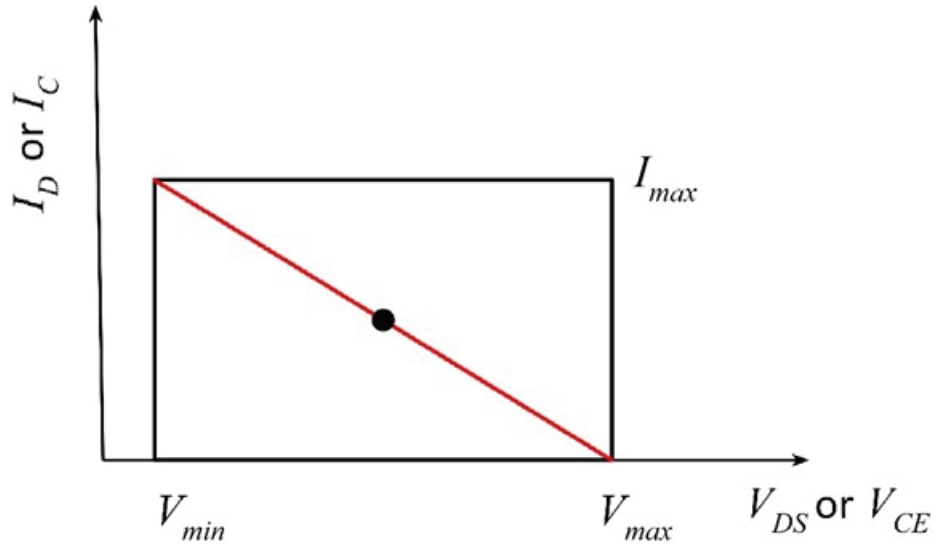
Transistors have resistive, capactive parasitics.

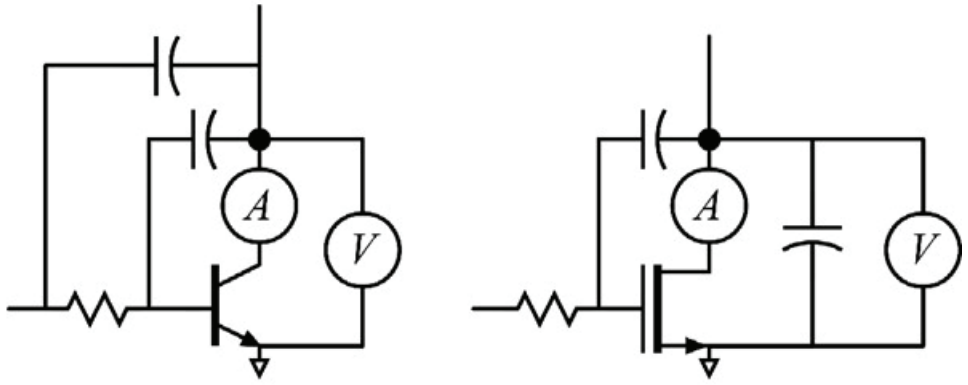
It is the *internal* (I_C, V_{CE}) or (I_D, V_{DS})
that must follow this loadline →

Loadline current must be electron current,
not $C \cdot dV / dt$ displacement current.

→ Current meters must be placed inside the capactive parastics.

How do we do this ?

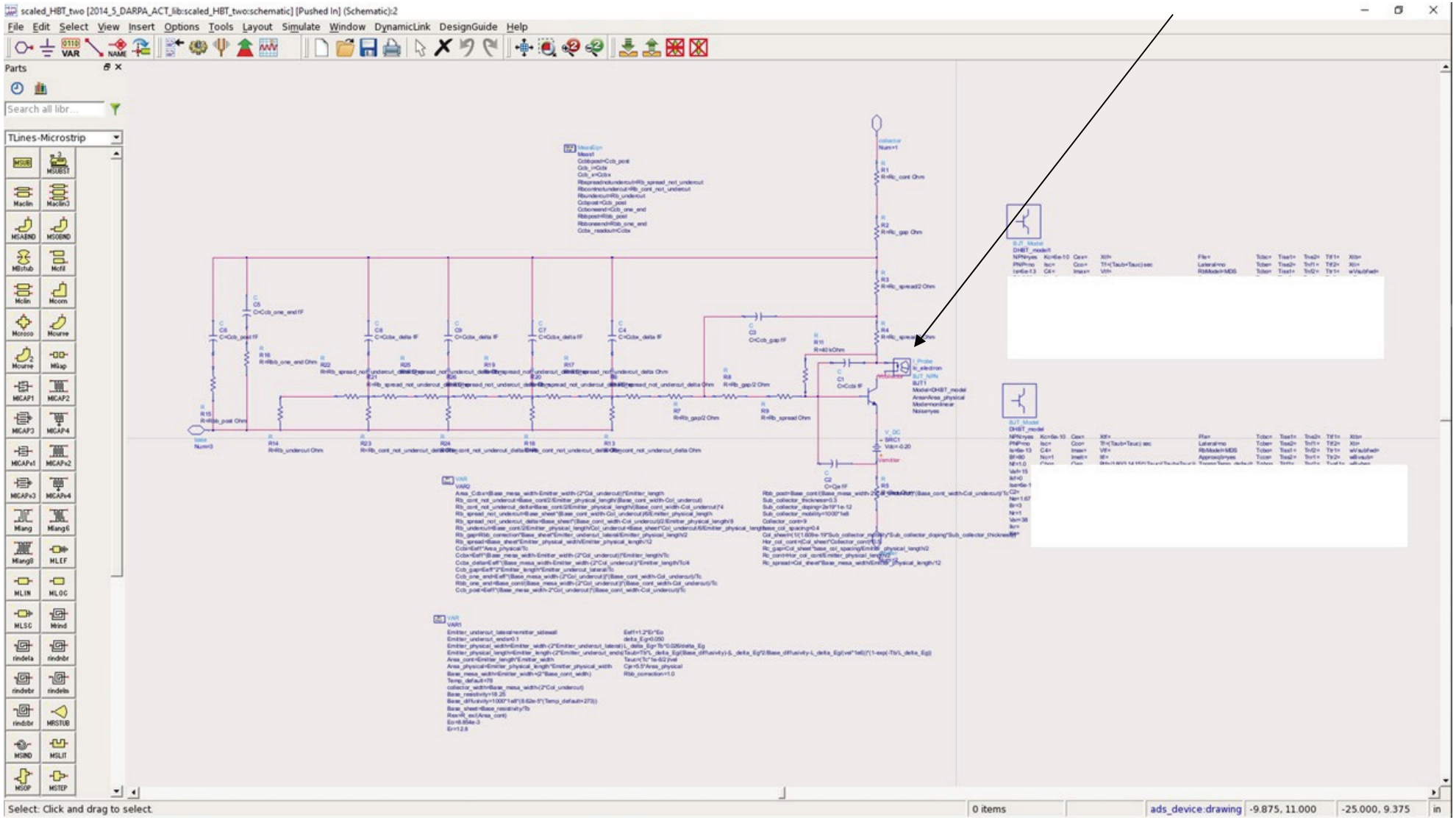




Loadline inclusive of transistor parasitics

If the transistor technology originates from the organization you work for, then CAD models may not be encrypted.

If so, you can edit the device CAD model to place an internal current meter.



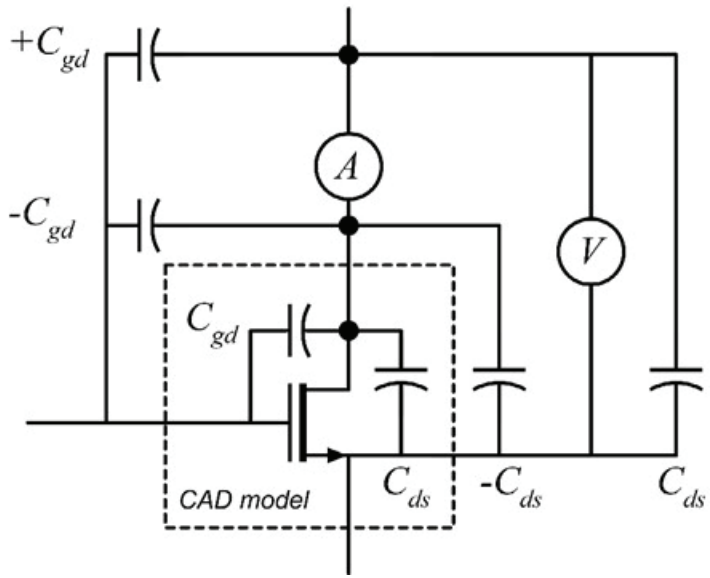
Loadline inclusive of transistor parasitics

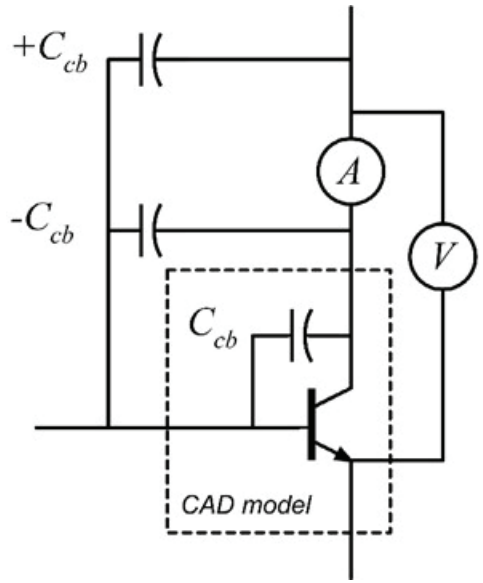
If the transistor technology does not originate
from the organization you work for,
then the CAD models may be encrypted.

If so

Use design kit CAD device model → simulate device S-parameters
From the S-parameters,
use established extraction procedures to determine transistor capacitances

Then, with transitor capacitances known:
1) add external negative capacitances to cancel these.
2) add voltmeter and current meter.
These correctly measure the loadline
3) then add back external positive capacitances.



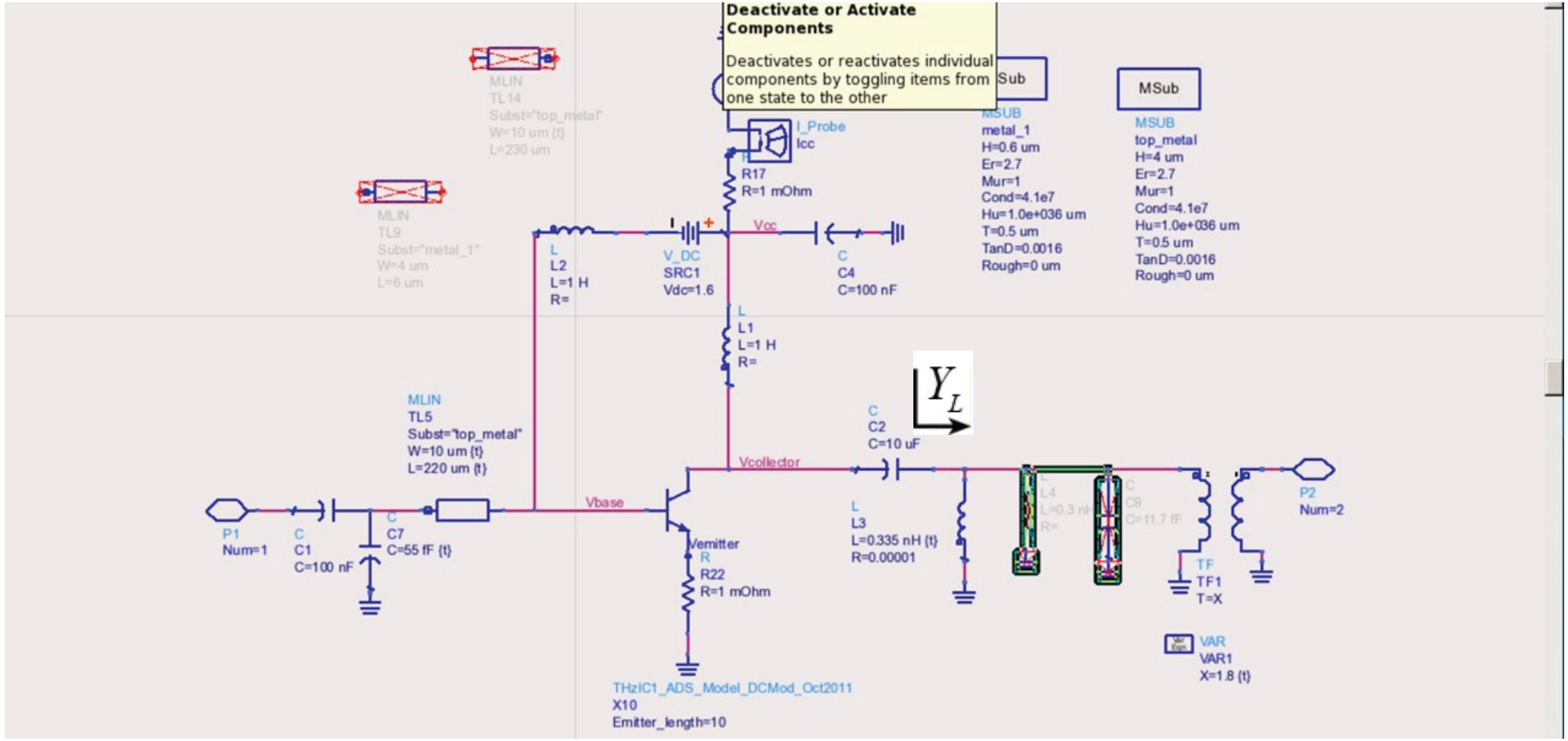


Power Amplifier Design Example

Power amplifier *cell*. 20 micron emitter finger. Bias: Ic = 10mA, Vcb = 1.86 Volts $\rightarrow V_{CE} = 2.5$ V.

The biasing technique used is just for CAD experimentation; (not practical bias circuit)

The inactivated output LC network is a bandpass filter



Power Amplifier Design Example

First, simulate the transistor S-parameters vs. frequency at the bias point

Determine:

f_{max},

stability factors, stability circles at the design frequency.

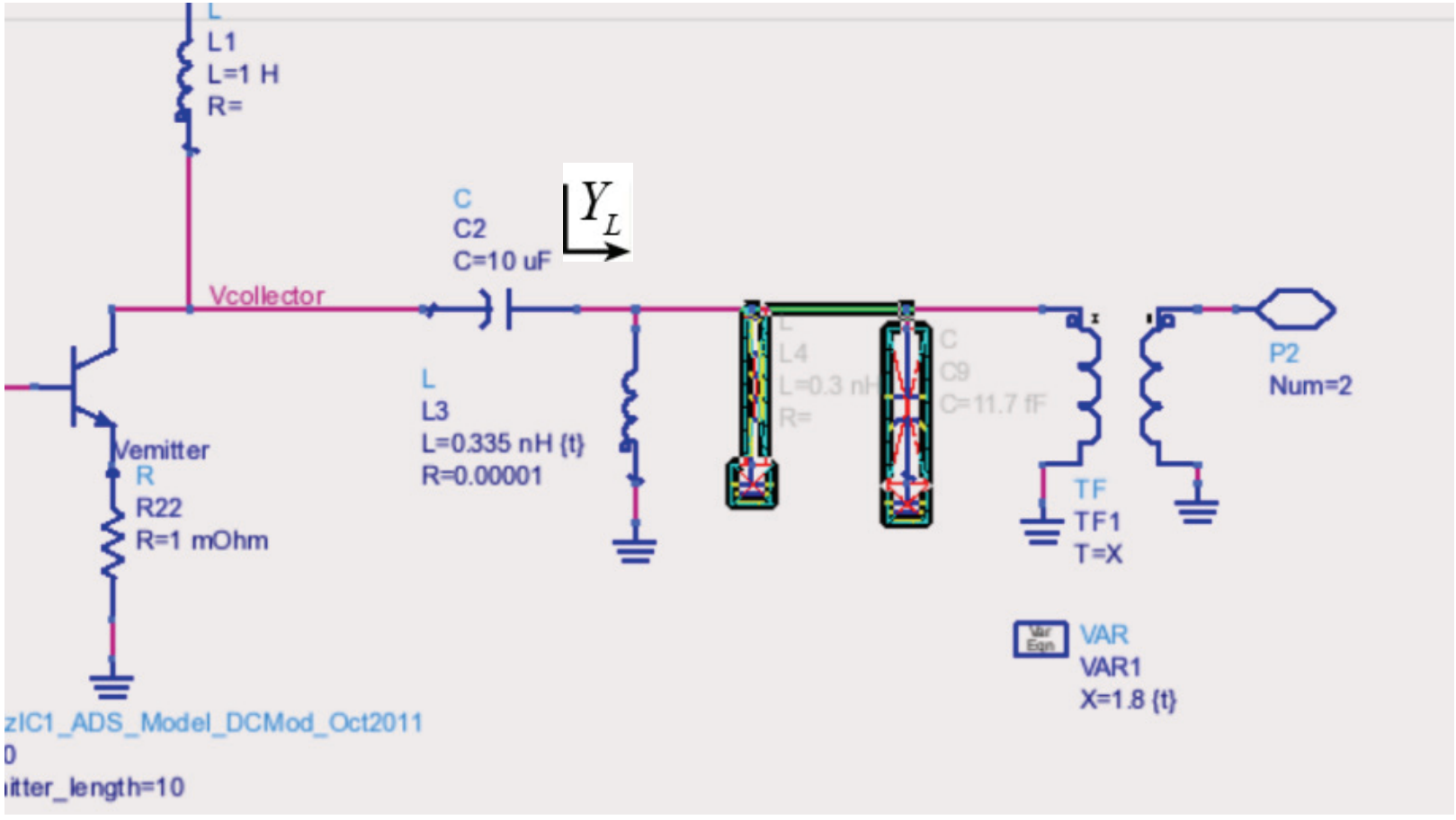
MAG/MSG at the design frequency.

If potentially unstable, stablize (input resistance or reactive feedback) at the design frequency

PA example: output network

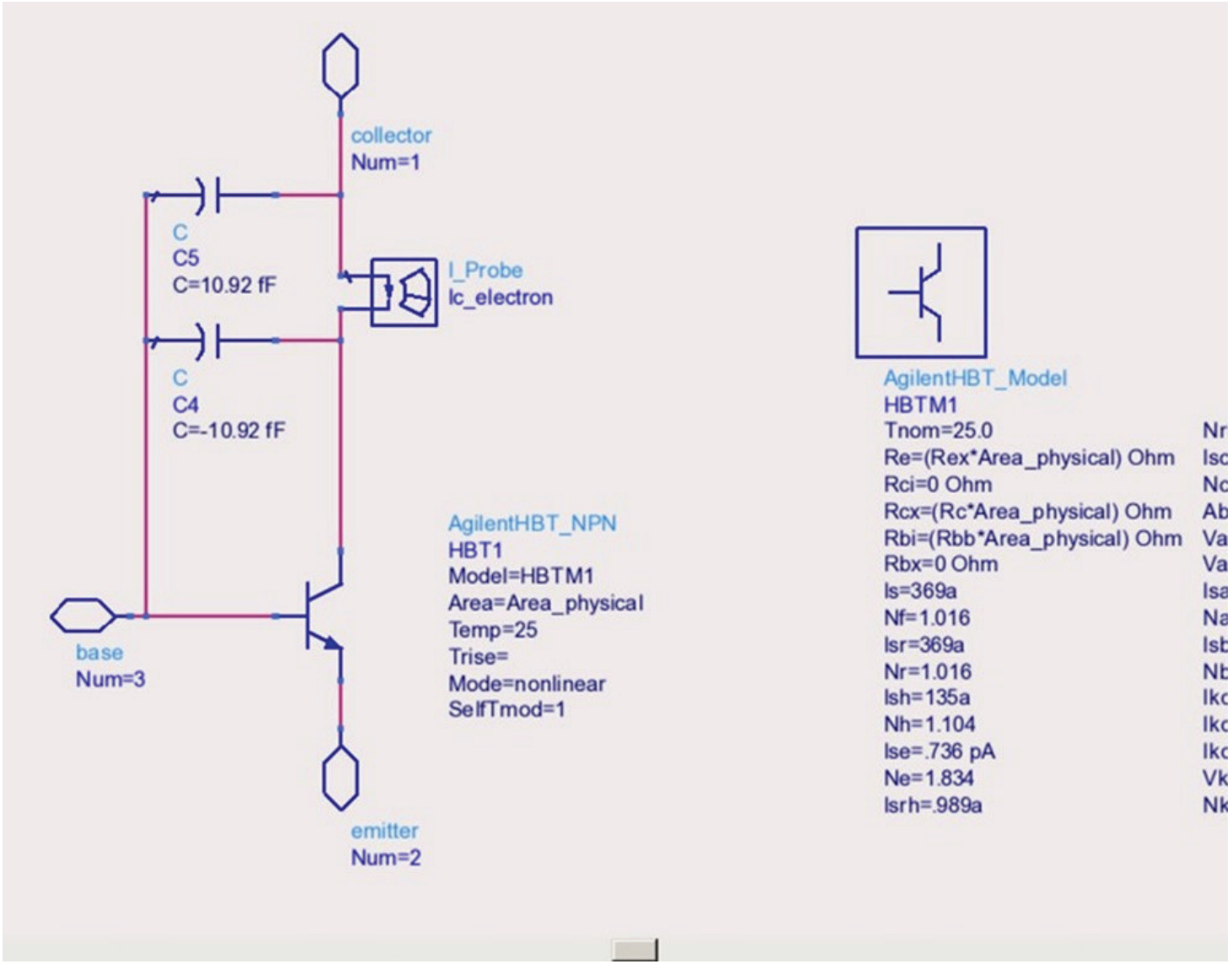
Note the output network: ideal transformer plus parallel inductance.

This is not the final ouput network: it is used to quickly find $Y_{L,opt}$.



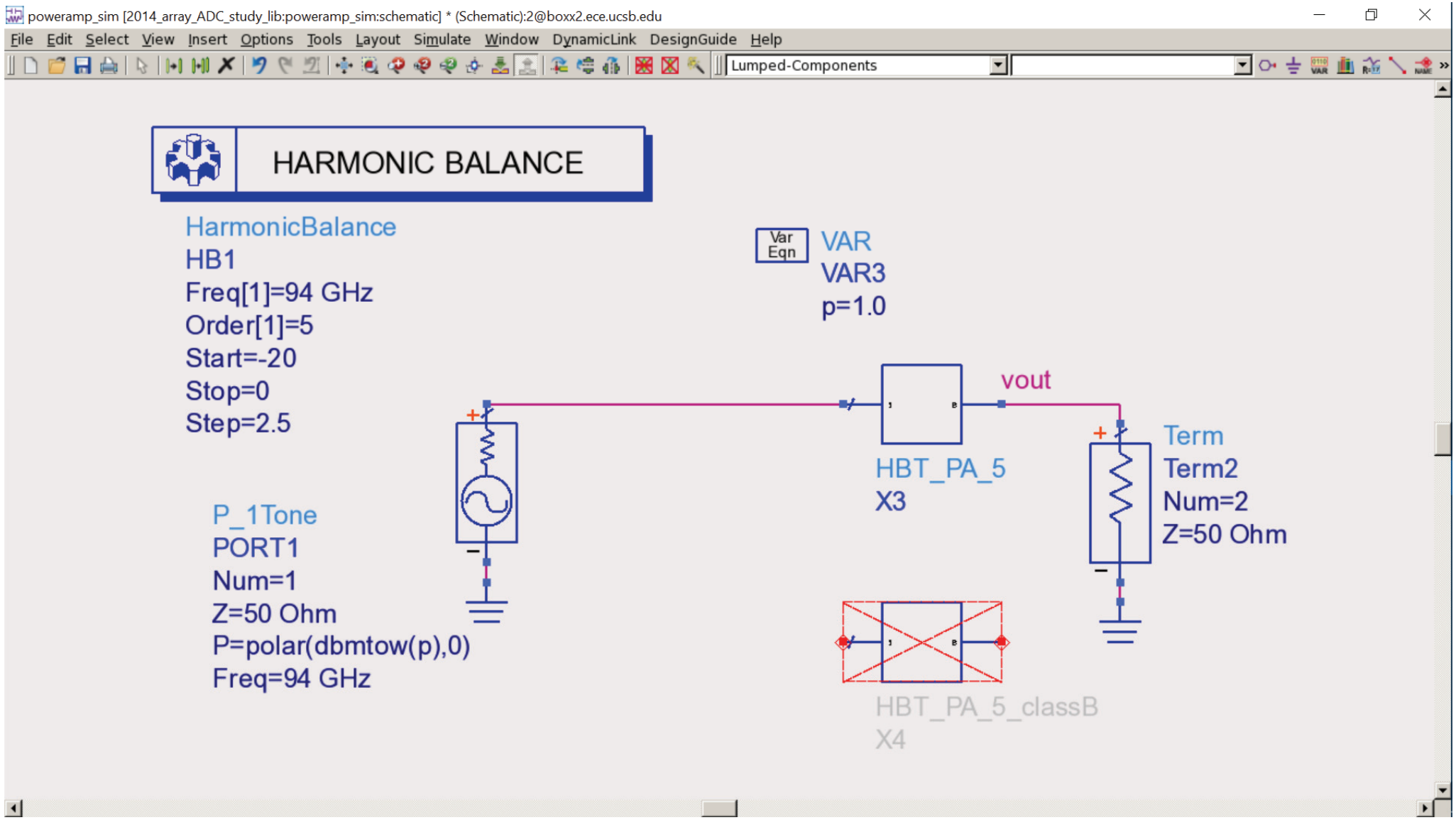
PA example: measuring the loadline

Dropping down in the heirarchy into the device model, we see the monitoring ammeter plus negative and positive C_{cb}.



PA example: finding the optimum load

The input is not yet matched, and the load is not yet tuned. We drive the transistor with a large drive signal and observe the loadline



Lissajous patterns

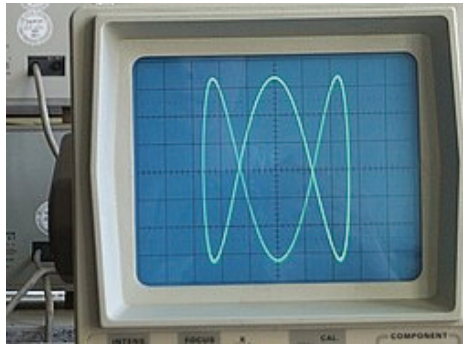
$x = A\cos(at+\theta)$

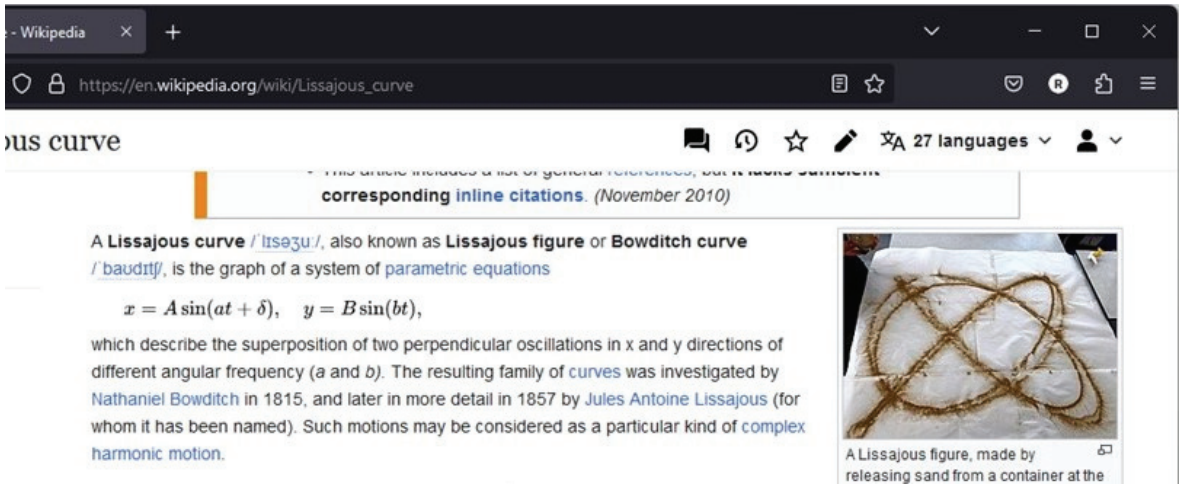
$y = B\cos(bt)$

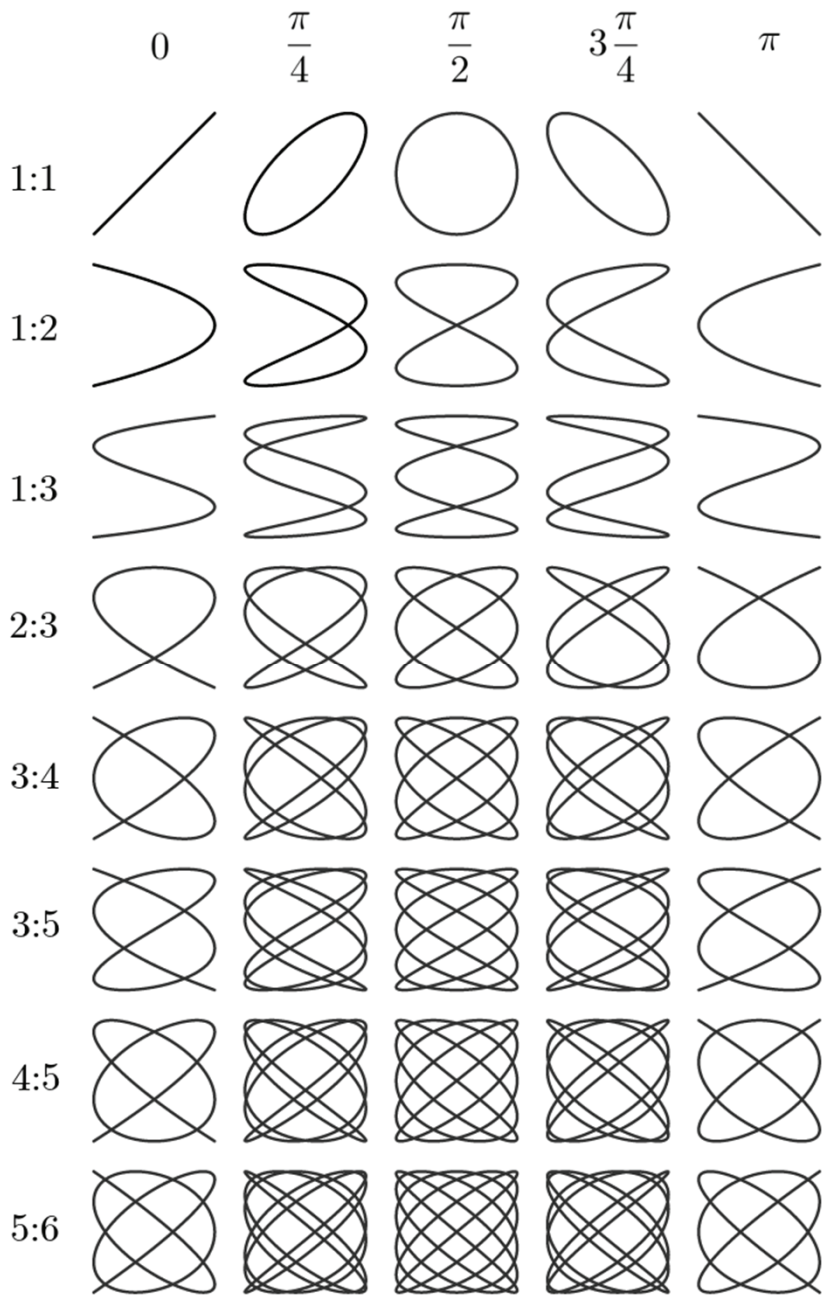
closed patterns if a/b is rational.

a/b or b/a sets # of loops.

for a=b, θ varies the curve beteen a line and an ellipse.





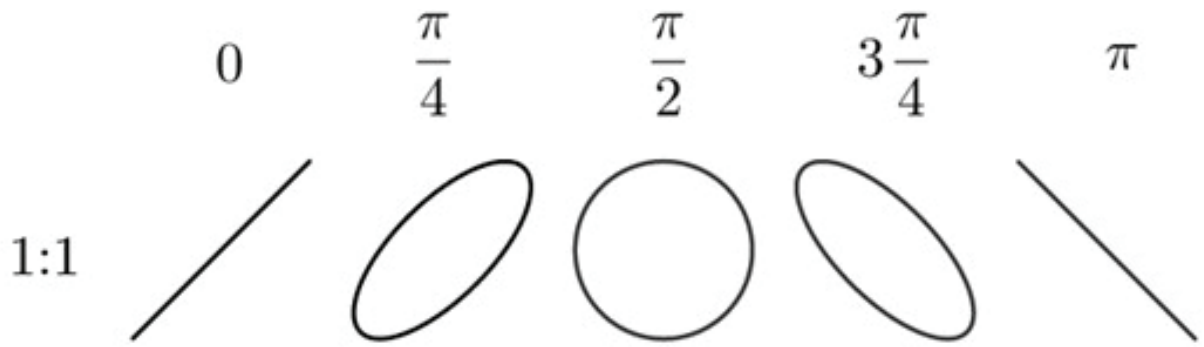


https://en.wikipedia.org/wiki/Lissajous_curve

https://en.wikipedia.org/wiki/Lissajous_curve#/media/File:Lissajous_relaciones.png

Reactive load: I vs. V is ellipse in (V,I) plane.

$$V_{DS}(t) = V_{DC} + V_{peak}\cos(\omega t + \theta)$$
$$I_{D,\text{internal}}(t) = I_{DC} + I_{peak}\cos(\omega t)$$

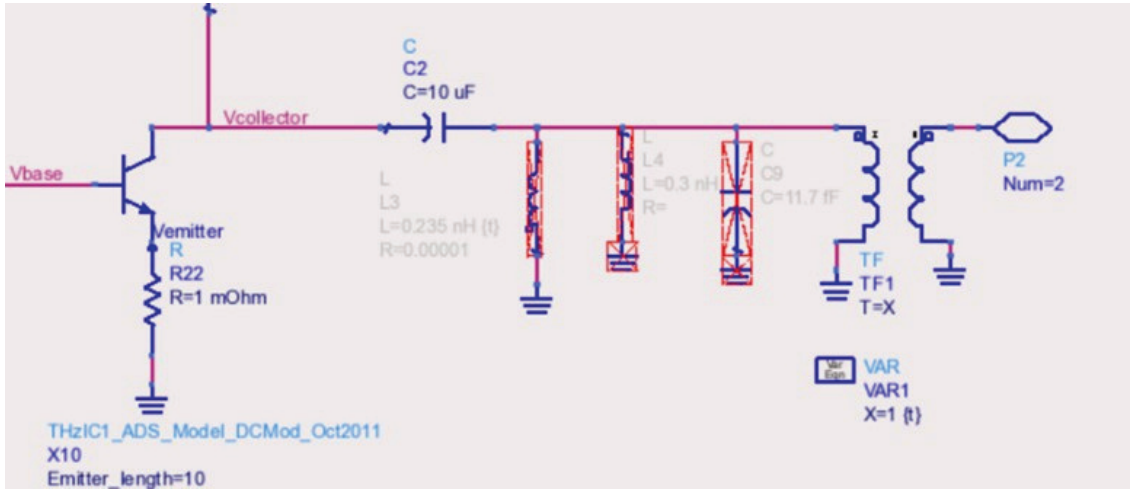


$\theta = 0^o$ or 180^o

$\rightarrow I_{D,\text{internal}}$ vs. $V_{DS,\text{internal}}$ is straight line in (V, I) plane

$\rightarrow Y_{L,\text{internal}} = (I_{peak}/V_{peak})\exp(-j\theta) = G_{L,\text{internal}} + jB_{L,\text{internal}}$

$Y_{L,\text{internal}} = G_{L,\text{internal}} + j0$ S is purely real admittance.



$\theta \neq 0^o$ and $\neq 180^o$

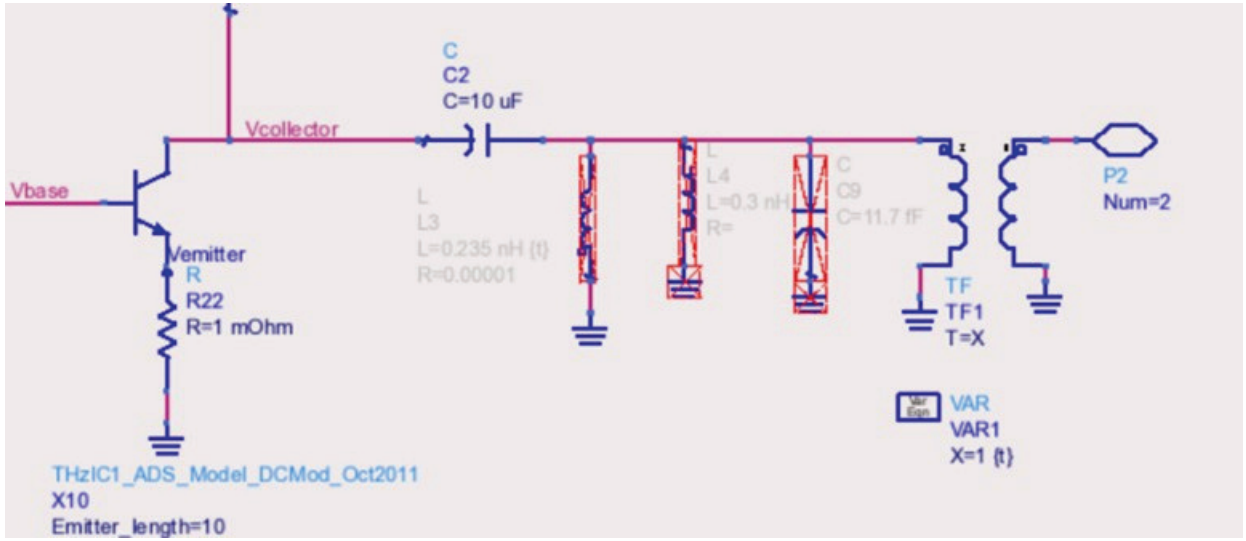
$\rightarrow I_D$ vs. V_{DS} is ellipse in (V, I) plane

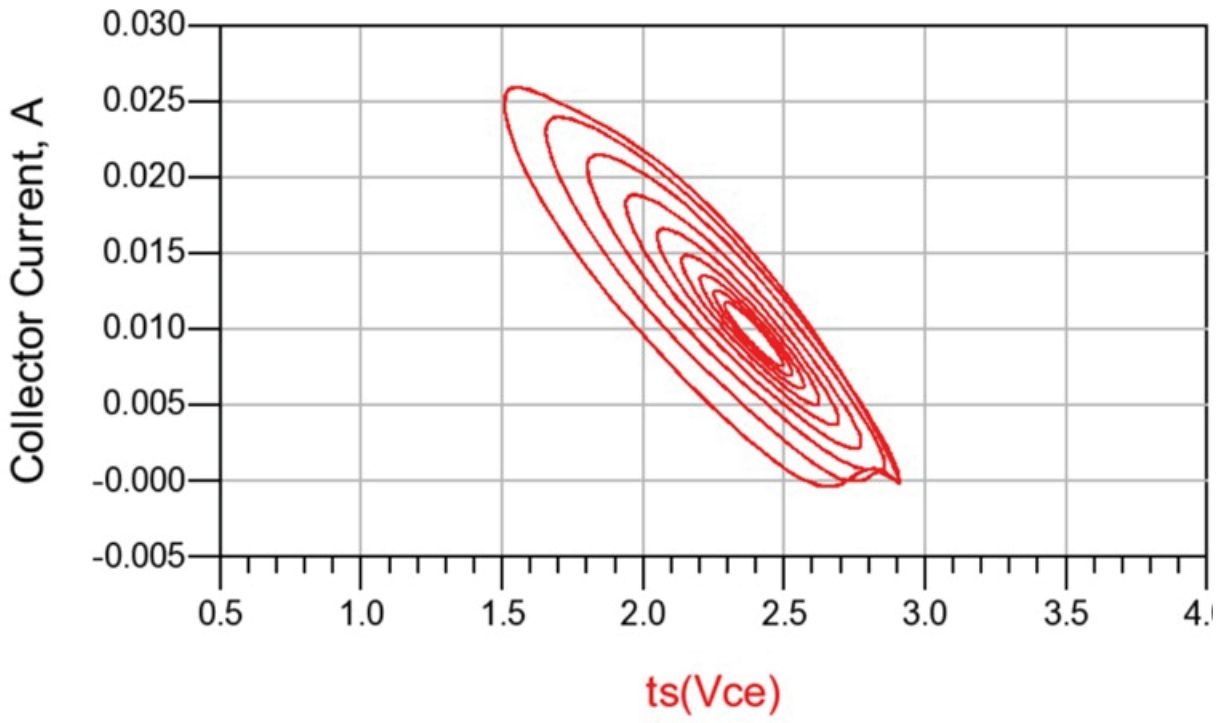
$\rightarrow Y_{L,\text{internal}} = (I_{peak}/V_{peak})\exp(-j\theta)$

$Y_{L,\text{internal}} = G_{L,\text{internal}} + jB_{L,\text{internal}}$ with $B_{L,\text{internal}} \neq 0$ S ; nonzero load susceptance

Power Amplifier Design Example

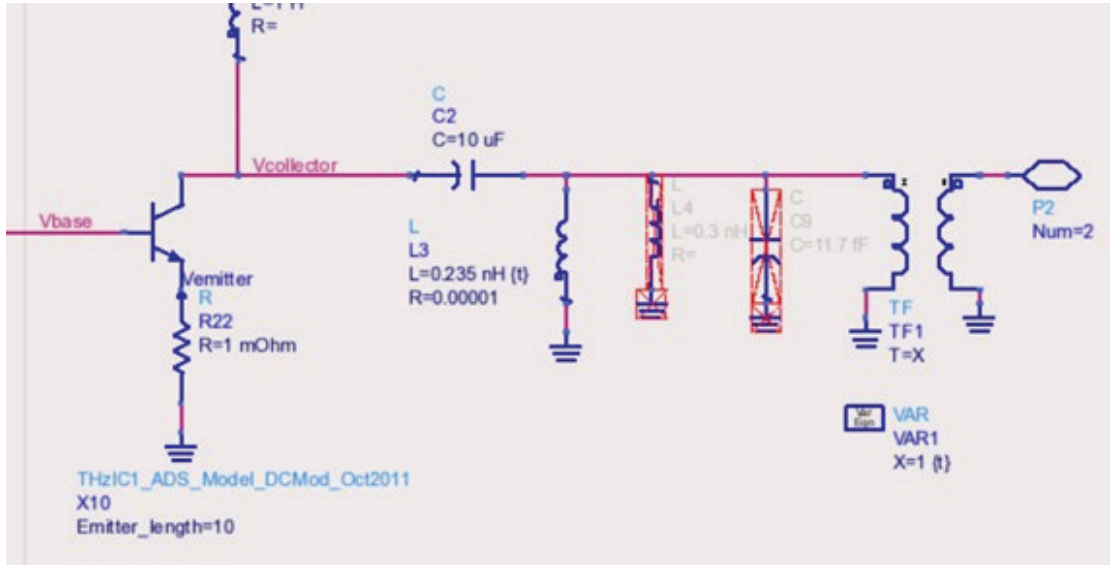
With no inductive tuning, and with a 1:1 transformer ratio, the loadline initially looks like this:

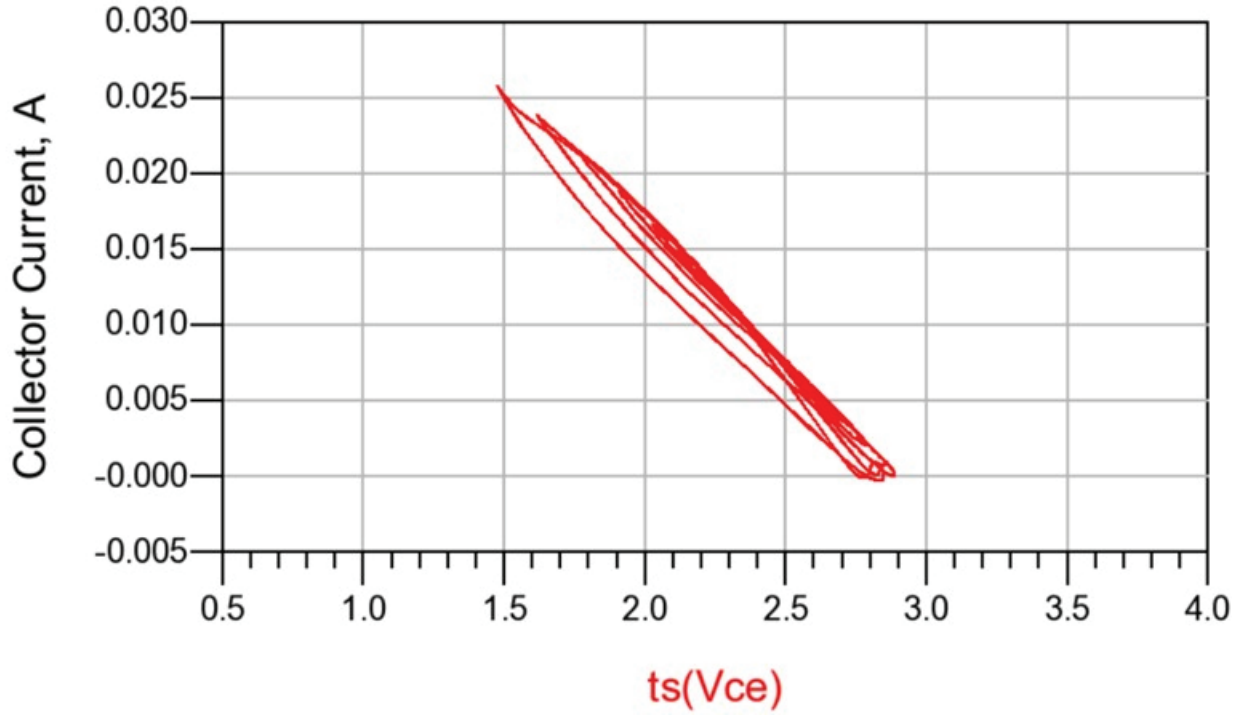




Power Amplifier Design Example

First add the inductive tuning, adjusting the shunt inductance, L, to eliminate loadline looping

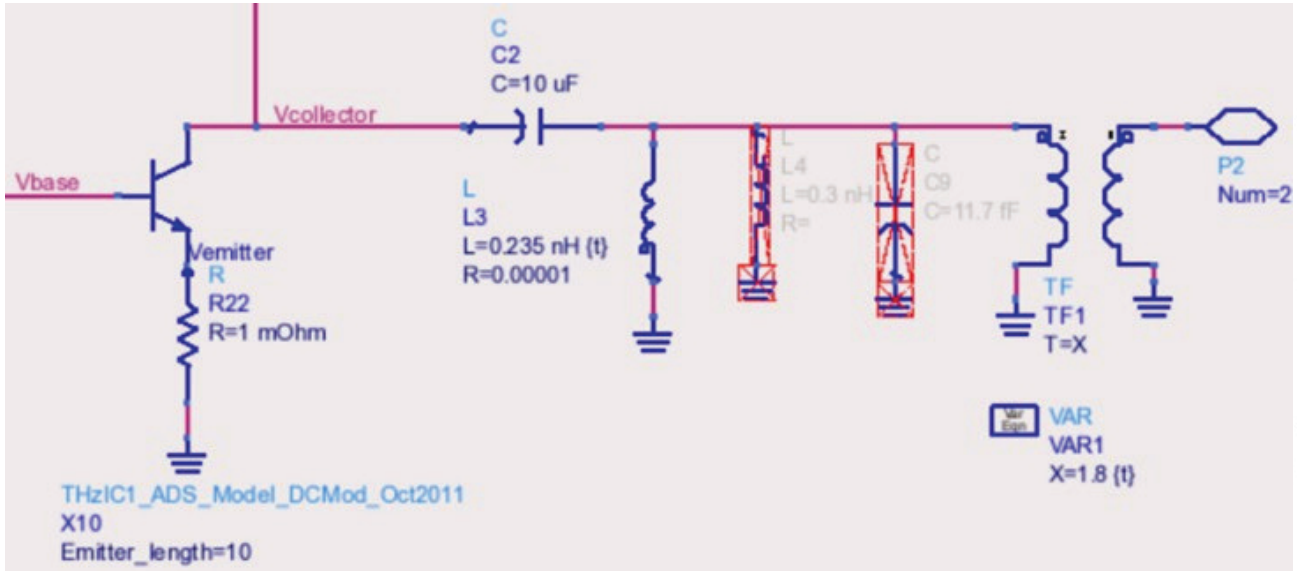


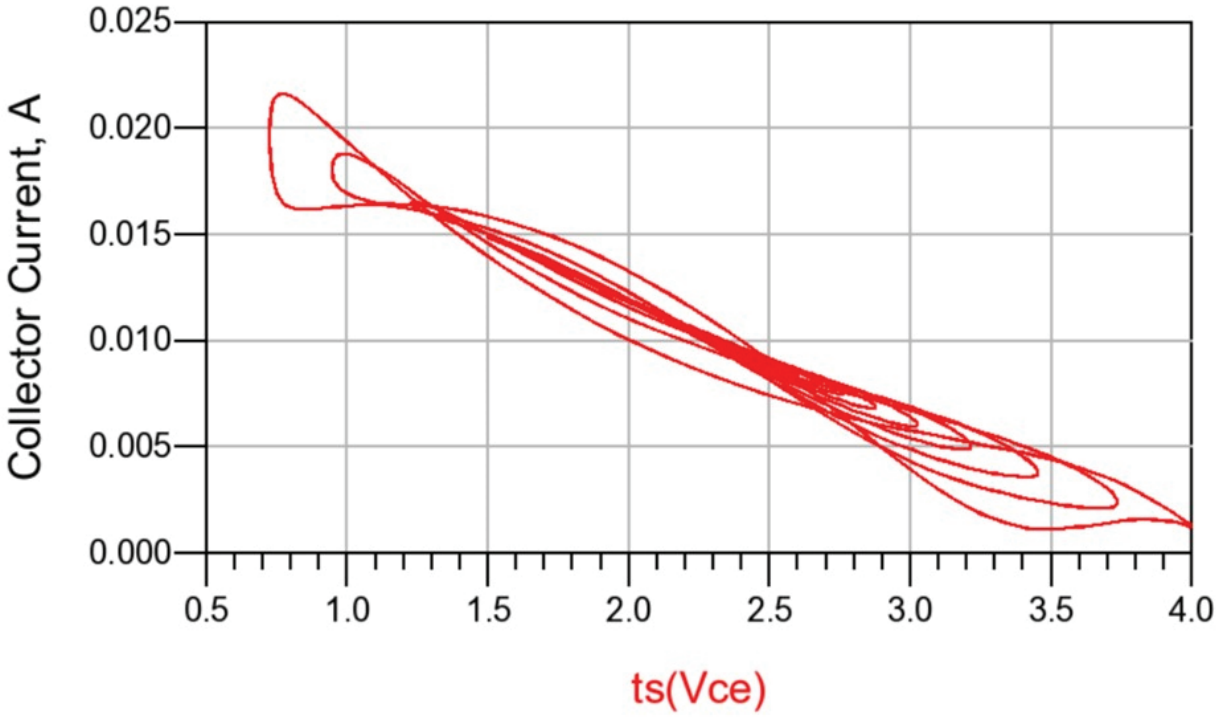


Power Amplifier Design Example

Then adjust the transformer ratio to obtain a loadline passing through the target endpoints (V_{min}, I_{max}) and $(V_{max}, I_{min} = 0A)$

We had expected a straight line. The looping (3 per cycle) is 3rd harmonic generation (consider again the Lissajous patterns)





Power Amplifier Design Example

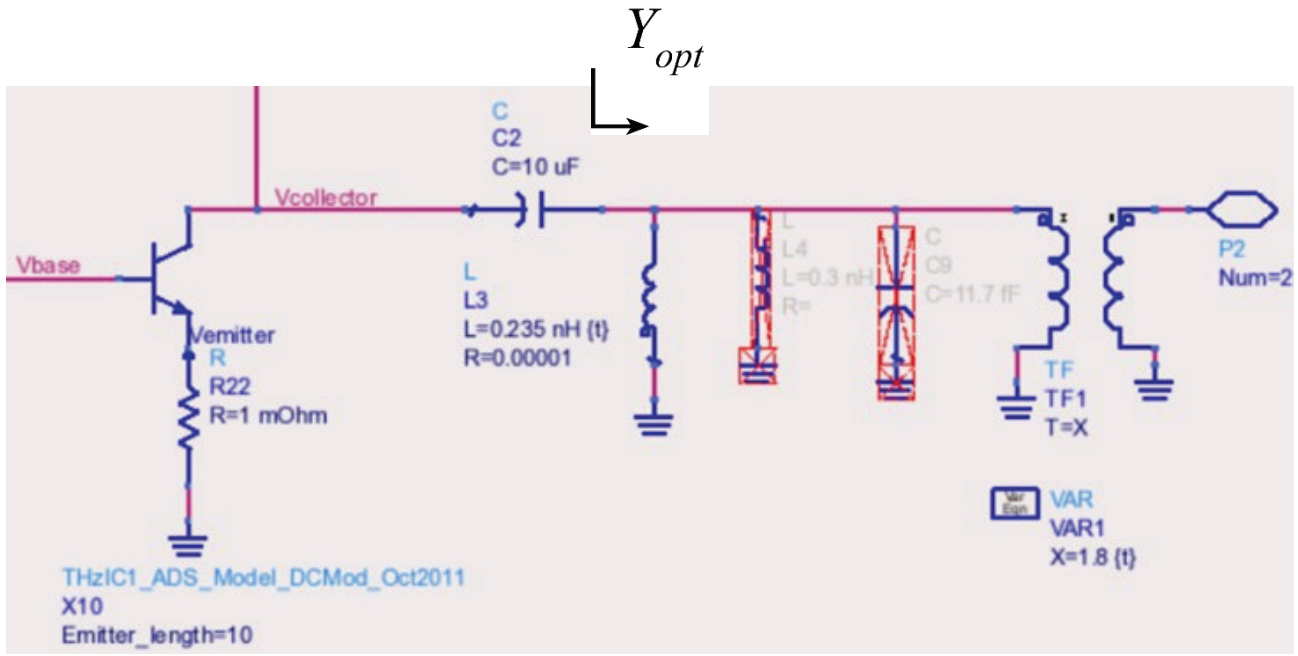
We have now determined Y_{opt}.

In this example:

$$Y_{opt} = \frac{1}{j\omega L} + \left(\frac{1}{\text{transformer turns ratio}} \right)^2 \frac{1}{50\Omega}$$

$$= \frac{1}{j\omega L} + \left(\frac{1}{X} \right)^2 \frac{1}{50\Omega}$$

$$= \frac{1}{j \cdot 2\pi \cdot 94\ \text{GHz} \cdot 0.235\ \text{nH}} + \left(\frac{1}{1.8} \right)^2 \frac{1}{50\Omega}$$

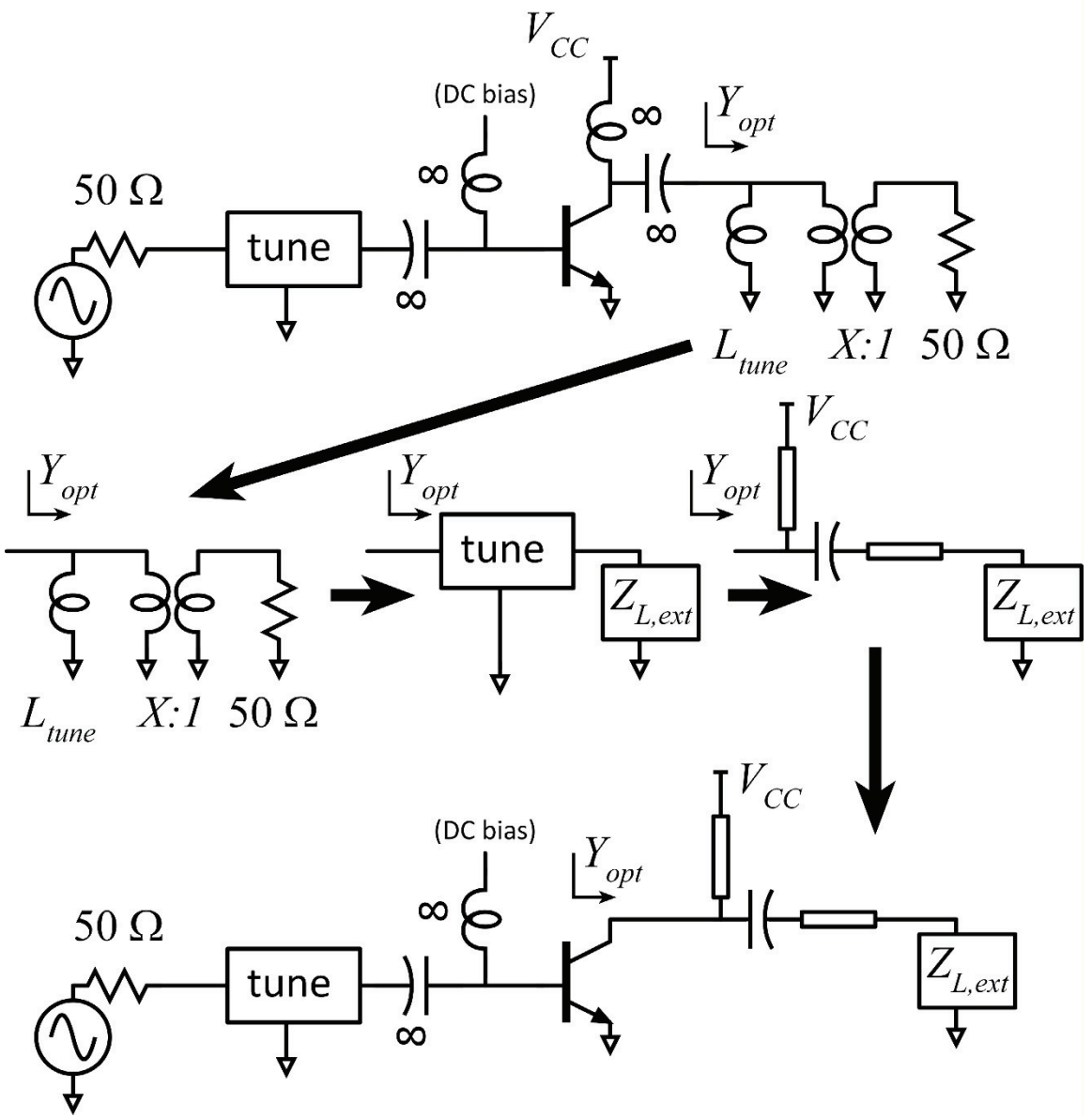


Power Amplifier Design Example

With Y_{opt} now determined,

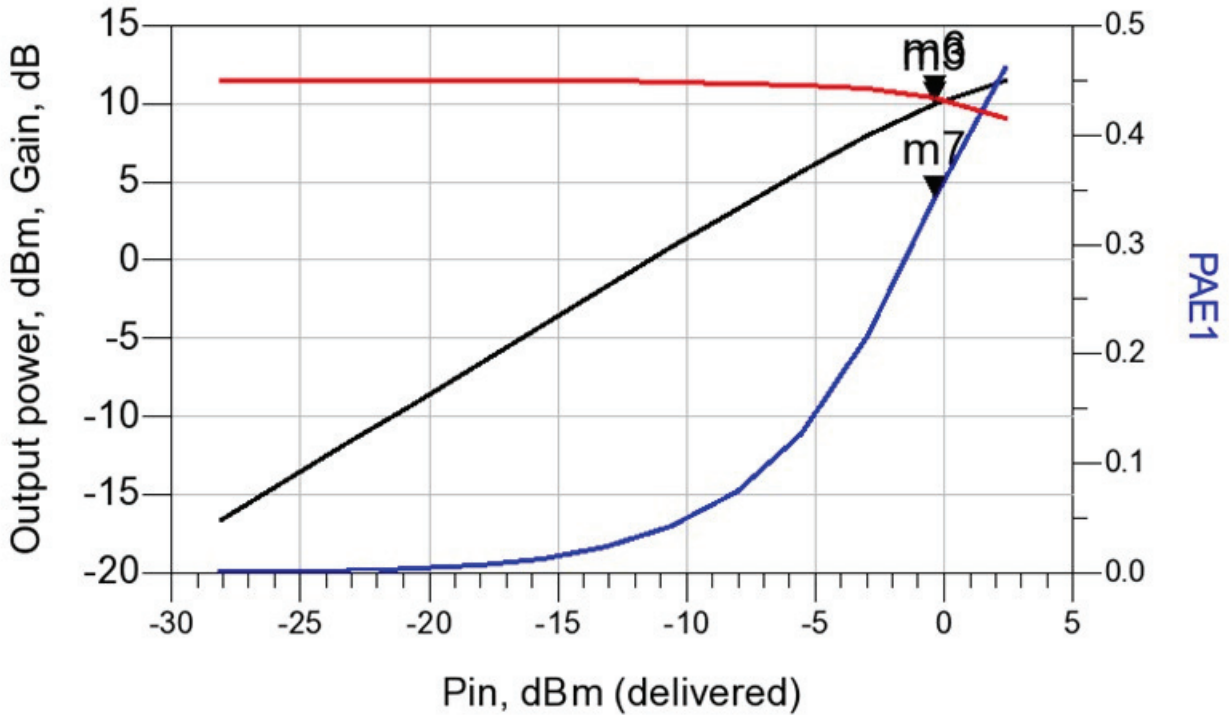
We then design a practical output network which that provides this Y_{opt}.

We then add this to the PA.



Power Amplifier Design Example

Here is our final simulated performance



m6
indep(m6)=-0.394
plot_vs(pout-Pin_deliv_dBm, Pin_deliv_dBm)=10.379

m7
indep(m7)=-0.394
plot_vs(PAE1, Pin_deliv_dBm)=0.342

m3
indep(m3)=-0.394
plot_vs(pout, Pin_deliv_dBm)=9.985

Other issues:

Input matching network

Out-of-band stabilization

(ece145a)

Often: filters

to suppress 2nd, 3rd harmonics.

Load pull method

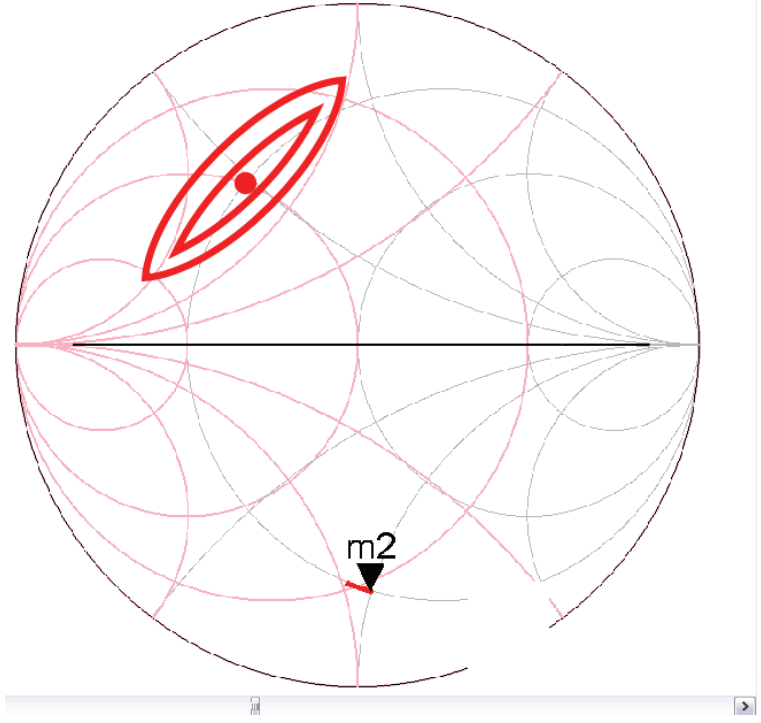
We can also empirically determine (in CAD, or with instruments) the load impedance giving the largest saturated P_{out}.

We then use this impedance for our PA design

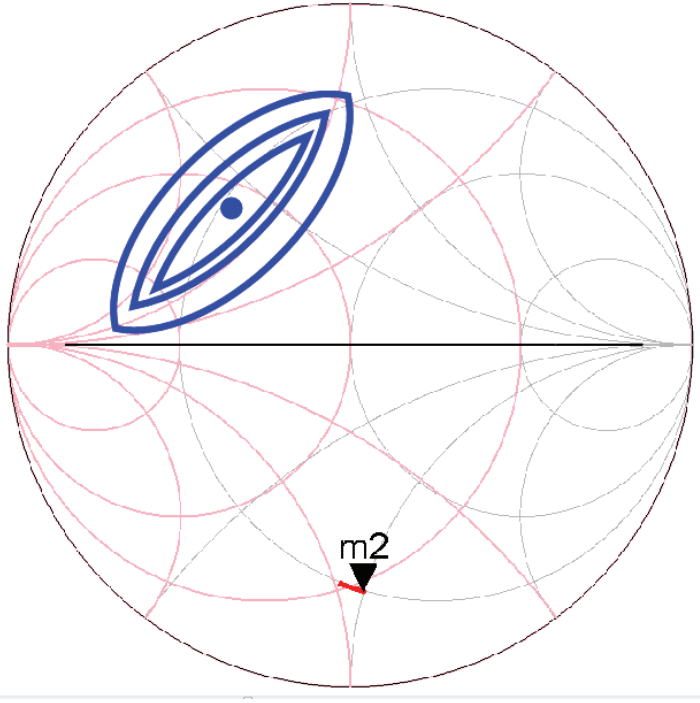
Empirical method. Simply contour plots of maximum P_{out} and peak PAE

Steven Cripps has a paper that shows that these contours are sets of intersecting ellipses on the Smith chart.

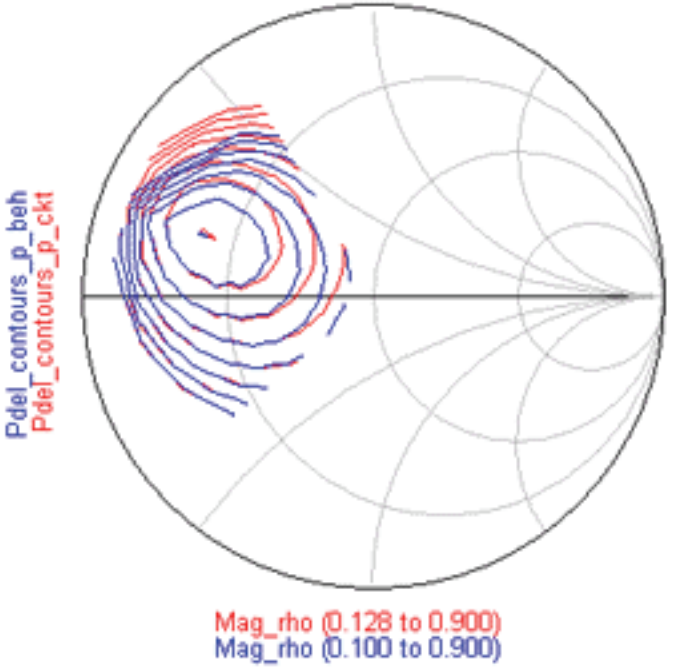
P_{sat} contours



PAE contours



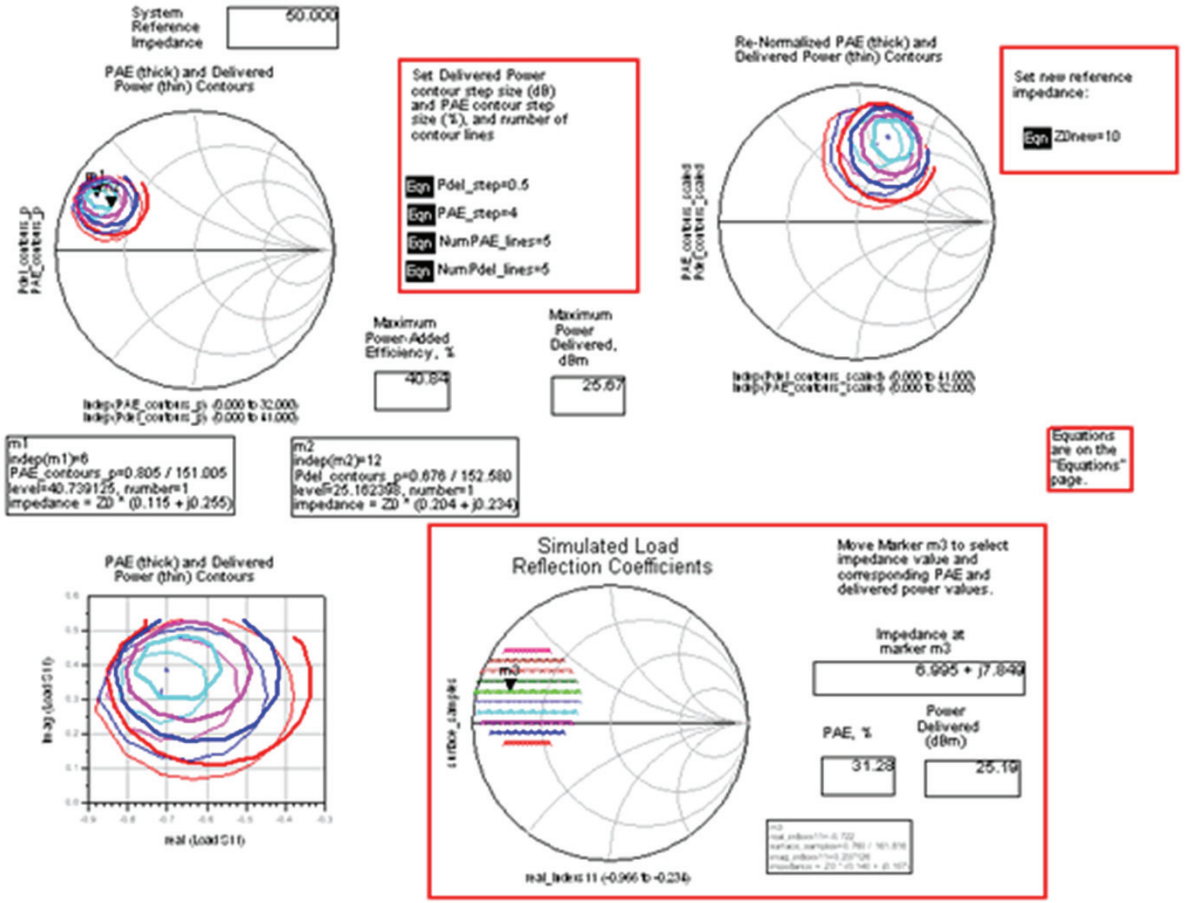
Keysight ADS plot

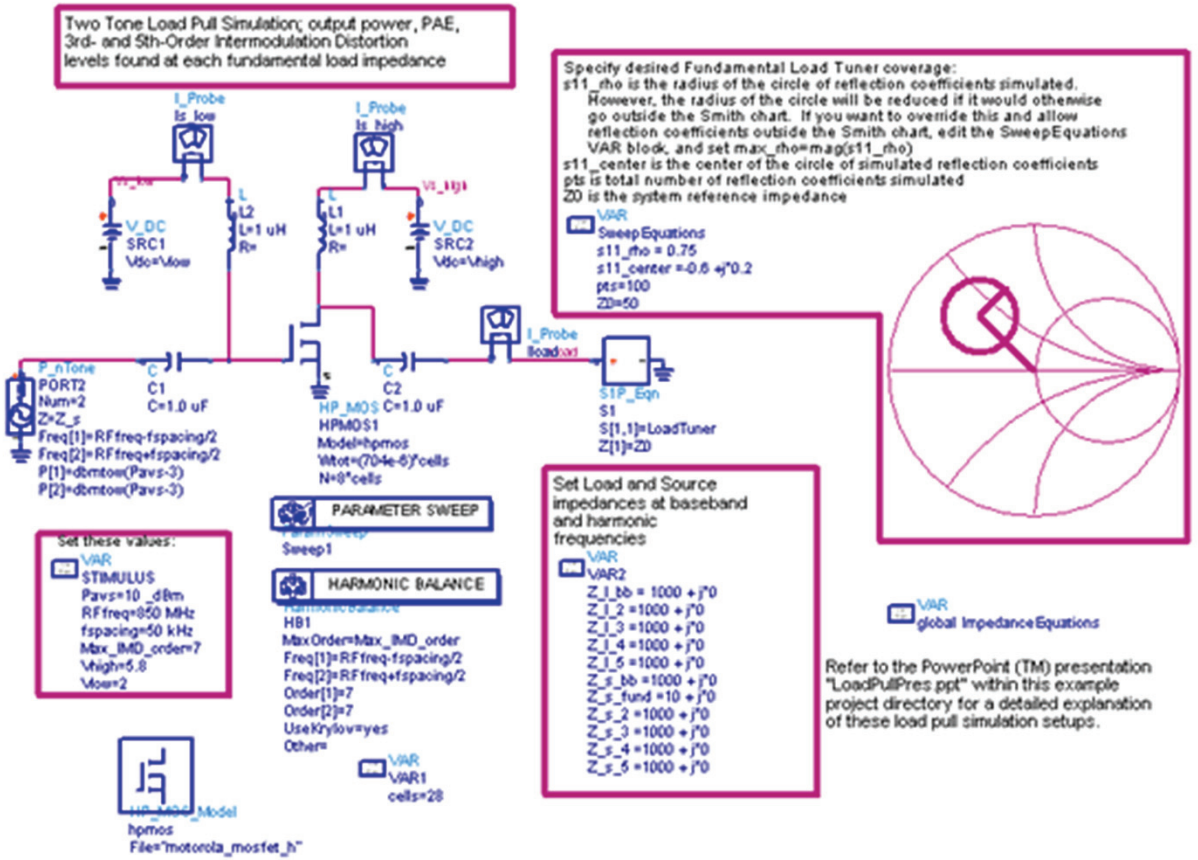


Load pull method

We can also empirically determine (in CAD, or with instruments) the load impedance giving the largest saturated P_{out}.

We then use this impedance for our PA design. Keysight ADS and other CAD packages have pre-configured test benches to do this.





What about the input network ?

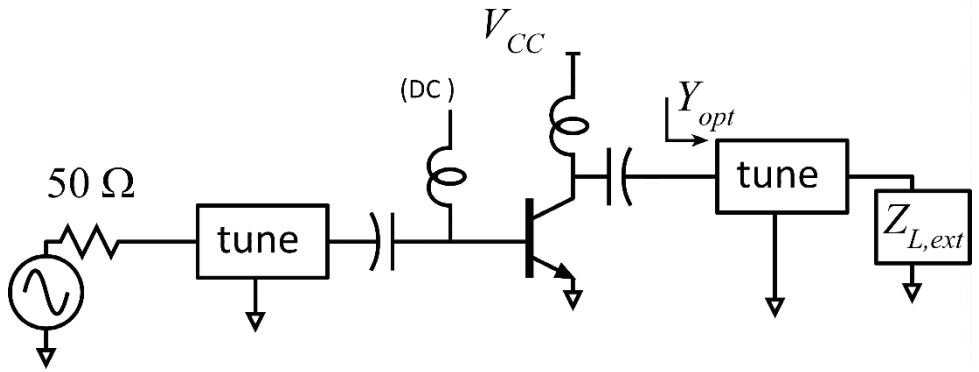
Thus far, we have considered only the output tuning network.

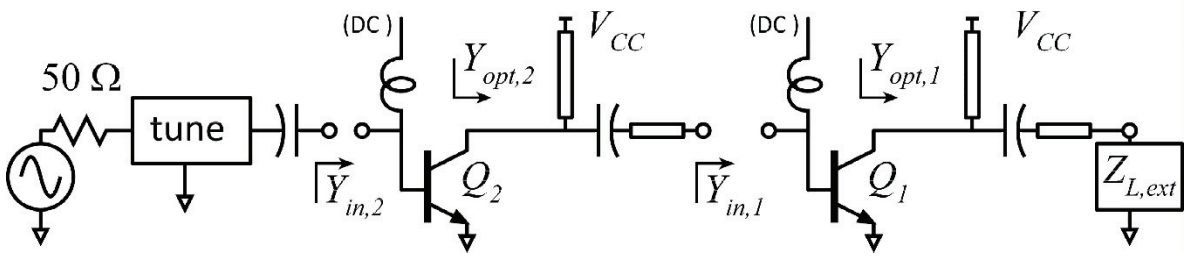
What about the input tuning network ?

To answer this, consider a multi-stage power amplifier.

Each cascaded stage, to be most efficient, must be loaded in its own optimum impedance

The input matching network design of Q_1 is now clear.





Considering a multi-stage power amplifier however immediately raises other concerns...

Multi-stage power amplifiers: power distribution

Assume for Q_1 :

@ $P_{out1} = 0$ dBm (small signal), $P_{in1} = -12$ dBm (12 dB gain) and PAE is low.

@ $P_{out1} = 17$ dBm, $P_{in1} = 6$ dBm (11 dB gain; 1 dB compression) and PAE=20%

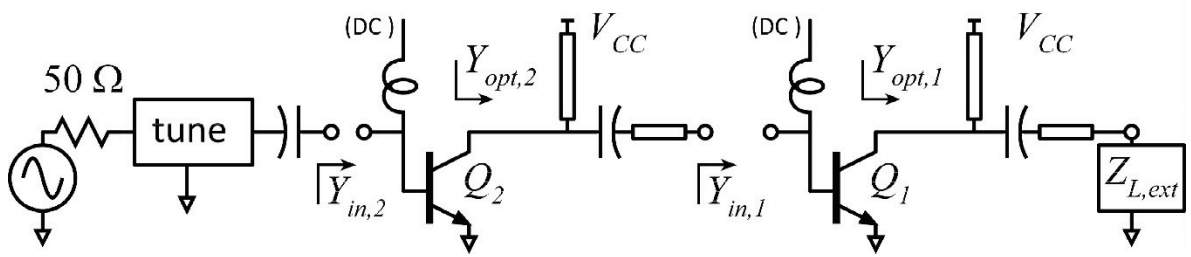
@ $P_{out1} = 20$ dBm, $P_{in1} = 10$ dBm (10 dB gain; 2 dB compression) and PAE=PAE_{MAX}=30%

Design for maximum overall PAE:

both stages must simultaneously operate at peak PAE.

→ Q_2 must reach peak PAE with $P_{out2} = 10$ dBm.

→ $A_{E2} = A_E / 10$



→ @$P_{out2} = 10$ dBm, $P_{in2} = 0$ dBm (10 dB gain) and PAE=PAE_{MAX}=30%

→ @ $P_{out2} = 0$ dBm (small signal), $P_{in2} = -12$ dBm (12 dB gain) and PAE is low.

2-stage amplifier:

@ $P_{out1} = 20$ dBm, $P_{in2} = 0$ dBm (20 dB total gain); 30% PAE for each stage; 30% overall PAE

@ $P_{out1} = 0$ dBm (small signal), $P_{in2} = -24$ dBm (24 dB gain).

4 dB gain compression between small-signal and peak PAE

Multi-stage power amplifiers: driver stage sizing

Assume for Q_1 :

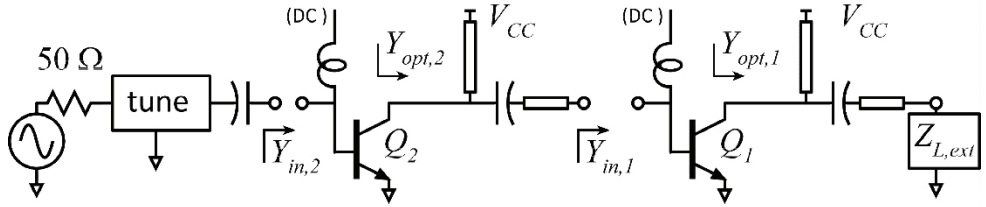
@ $P_{out1} = 0$ dBm (small signal), $P_{in1} = -12$ dBm (12 dB gain) and PAE is low.

@ $P_{out1} = 17$ dBm, $P_{in1} = 6$ dBm (11 dB gain; 1 dB compression) and PAE=20%

@ $P_{out1} = 20$ dBm, $P_{in1} = 10$ dBm (10 dB gain; 2 dB compression) and PAE=PAE_{MAX}=30%

Design for less gain compression:

size Q_2 such that Q_2 has 1 dB compression when Q_1 has 2 dB compression.



→ Q_2 must reach 1 dB gain compression with $P_{out2} = 10$ dBm.

→ $A_{E2} = A_E / 5$

→ @$P_{out2} = 10$ dBm, $P_{in2} = -1$ dBm (11 dB gain) and PAE=20%

→ @ $P_{out2} = 0$ dBm (small signal), $P_{in2} = -12$ dBm (12 dB gain) and PAE is low.

2-stage amplifier:

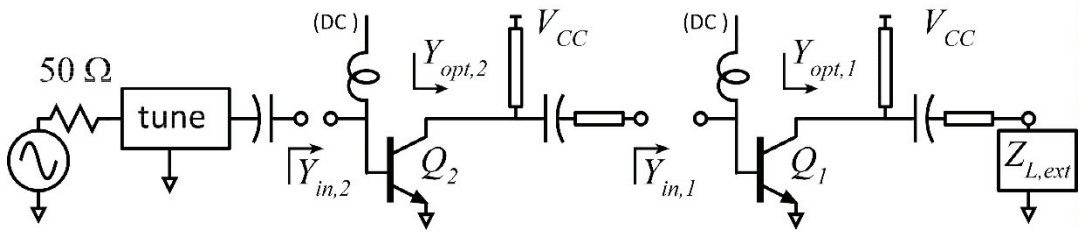
@ $P_{out1} = 20$ dBm, $P_{in2} = -1$ dBm (21 dB total gain); $PAE_1 = 30\%$; $PAE_2 = 20\% \rightarrow PAE_{overall} = (P_{out1} - P_{in2}) / (P_{DC1} + P_{DC2}) = 28.7\%$

@ $P_{out1} = 0$ dBm (small signal), $P_{in2} = -24$ dBm (24 dB gain).

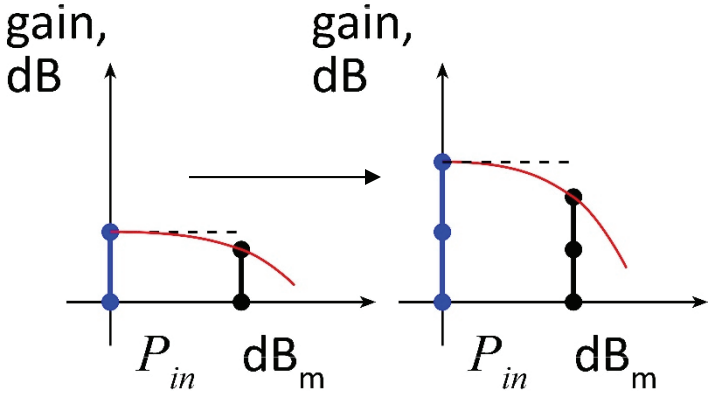
3 dB gain compression between small-signal and peak PAE

Over-sized driver stages

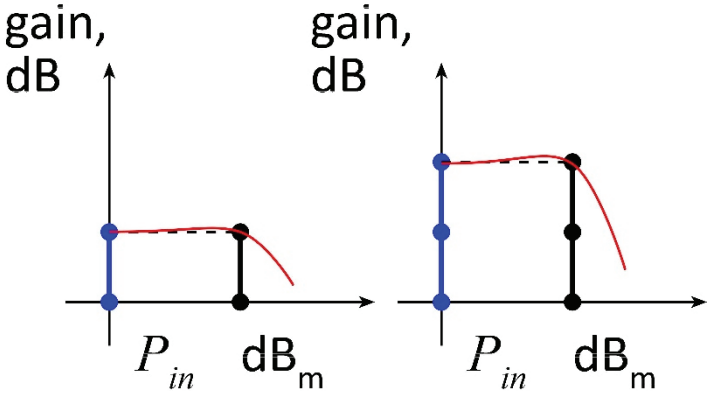
In a multi-stage amplifier, if driver stages are sized for peak PAE, then gain compression at PAE will increase rapidly as the number of stages is increased to increase the overall gain.



Over-sizing the driver stages will reduce the accumulated gain compression, but will reduce the overall PAE.



Adaptive bias circuits can be used in some systems to flatten the dB(P_{out}) vs. dB(P_{in}) characteristics.



Overall digital pre-distortion can also be applied.

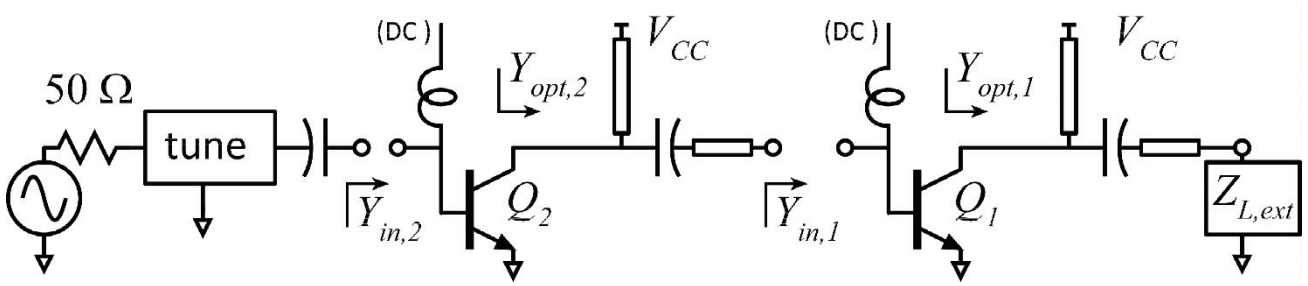
These are advanced topics, but important ones.

Multi-stage PAs: I_{max}, Z_{load}, transistor size problems

Consider this 2-stage amplifier:

$P_{out1} = 1000$ mW; $P_{in1} = 100$ mW;

$P_{out2} = 100$ mW; $P_{in2} = 10$ mW



Assume $(V_{max} - V_{min}) = 4$ Volts and recollect that

$Z_L = 1/Y_L = R_L + j0\Omega = (V_{max} - V_{min})/I_{max}$

$I_{DC} = I_{max}/2$

$P_{RF,max} = (V_{max} - V_{min})I_{max}/8 = (V_{max} - V_{min})^2/8R_L$

BJTs or FETs with $J_{max} =$ 2 mA/μm current density

Then

Stage 1: $I_{DC} = 1$ A; $R_L = 2\ \Omega$; $N_G W_G$ or $N_E L_E = 1000\ \mu$m

Stage 2: $I_{DC} = 100$ mA; $R_L = 20\ \Omega$; $N_G W_G$ or $N_E L_E = 100\ \mu$m

Extremely low load impedances, extremely high currents,extremely large transistor sizes.

This is the microwave power-combining problem