

ECE 145C / 218C, notes set xx: Class A Power Amplifiers

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Class A power amplifier

Class A: amplifier that is at least nominally linear for small to moderate-amplitude input signals.

Clearly clips (limits) for large output voltages.

Maximum voltage V_{\max}

Minimum voltage V_{\min}

Maximum current I_{\max}

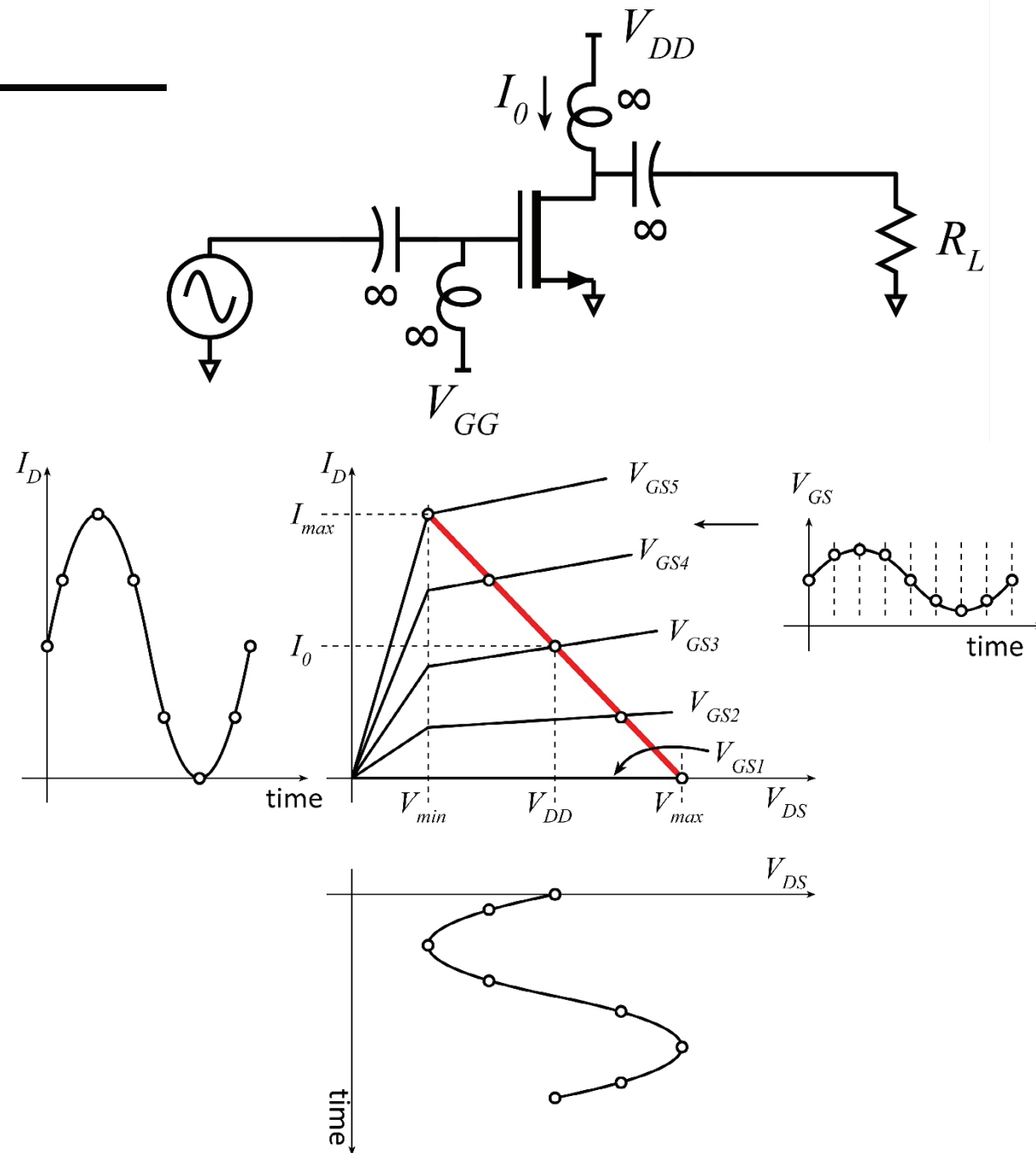
Bias drain current I_0

Bias drain voltage V_{DD}

If FET $I - V$ characteristics were linear then

$$I_0 = I_{\max} / 2; V_{DD} = (V_{\max} - V_{\min}) / 2.$$

...but real transistors are not perfectly linear



Transistor Output Characteristics

Idealized:

Minimum voltage: V_{knee}

Maximum voltage: V_{br}

Maximum current: I_{max}

FETs: $I_{max} \propto (\text{gate width})(\# \text{ gate fingers}) = N_g W_g$,

bipolars: $I_{max} \propto (\text{emitter length})(\# \text{ emitter fingers}) = N_e L_e$

Real

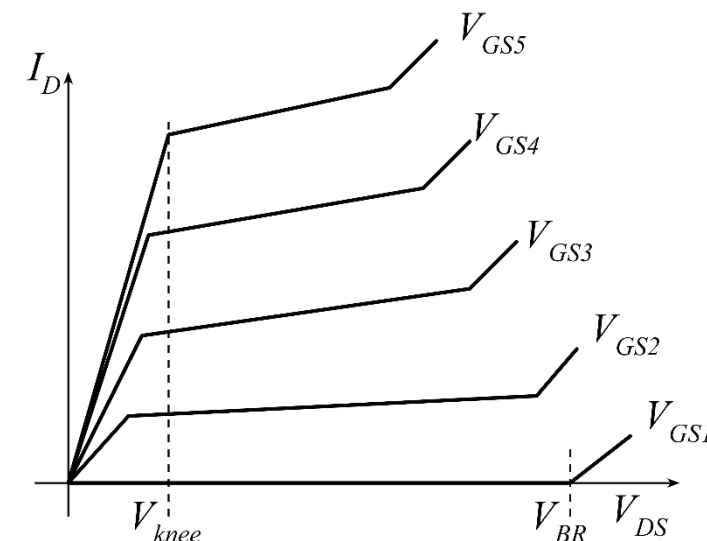
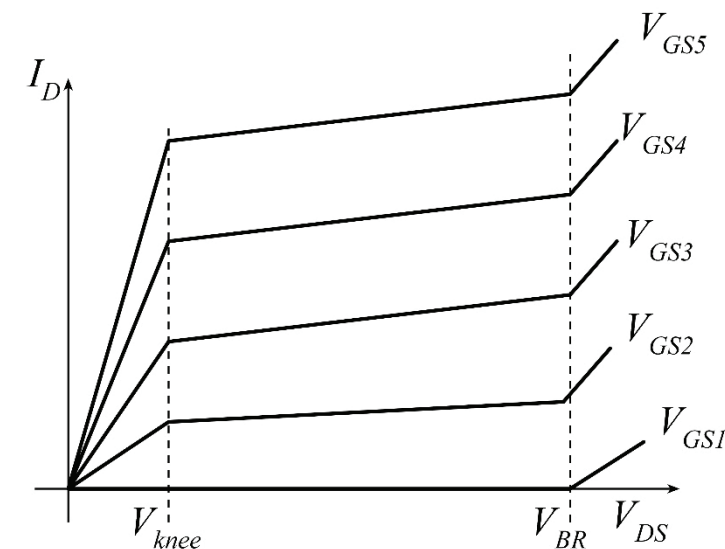
V_{br} depends on I_D or I_C

V_{knee} depends on I_D or I_C

Comments/Caution

Textbooks: $V_{knee} = V_{sat}$; Reality V_{knee} due to many factors

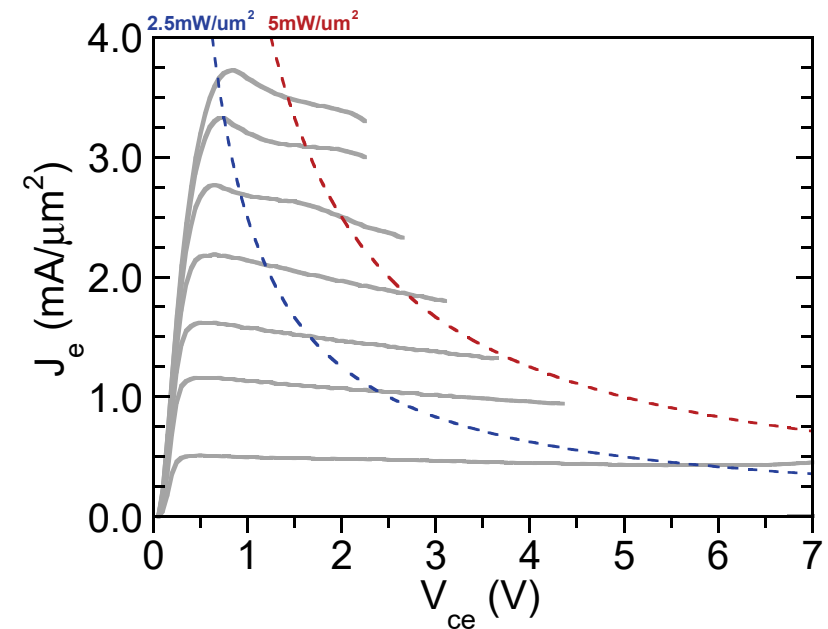
Textbooks: bipolar $V_{BR} = V_{BRCBO}, V_{BRCEO}$ etc. ; Reality is much more complicated.



Transistor Output Characteristics: measured

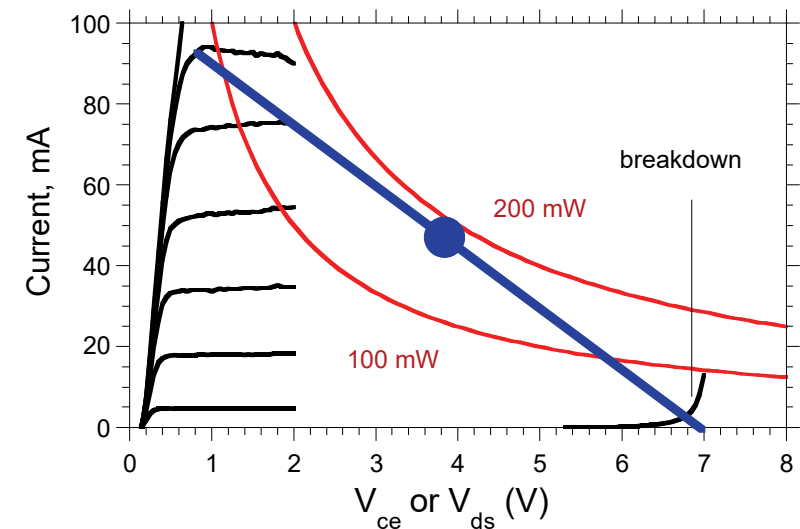
250nm InP HBT

$$\begin{aligned}
 I_E &= (\text{emitter current density})(\text{total emitter area}) \\
 &= J_E (\text{number emitter fingers})(\text{emitter area per finger}) \\
 &= J_E N_E A_E
 \end{aligned}$$



500nm InP HBT

(not sure what emitter area this is)



For I-V curves of state-of-art MOSFETs,
please see recent IEDM conference digests.

Transistor Output Characteristics: Instantaneous Power Contours

Instantaneous **dissipated** power = $V_{ce}I_c$ or $V_{DS}I_D$

Constant power contours: hyperbolas on I_{out}, V_{out} plane

Low-frequency power amplifier

signal frequency \ll (thermal time constant) $^{-1} = \tau_{\text{thermal}}^{-1}$

→ loadline must lie below maximum power density curve

τ_{thermal} can be of order of μs to ns, depending on transistor size.

High-frequency power amplifier

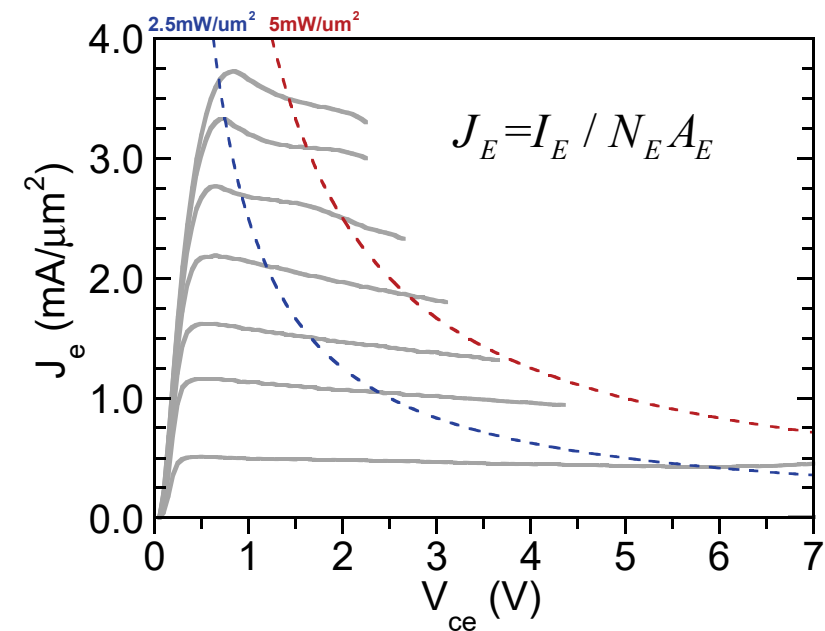
signal frequency \gg (thermal time constant) $^{-1}$

→ *bias point* must lie below maximum power density curve

Note: measured DC (I,V) characteristics are influenced by heating.

Breakdown with $f_{\text{signal}} \gg \tau_{\text{thermal}}^{-1}$ can be larger than V_{BR} @DC.

RF loadline can surpass DC breakdown voltage.



Transistor parameters and cutoff frequencies vary across (I,V) plane

Bipolar Transistors:

Low voltage and high current:

"Kirk effect" = space-charge-limited current

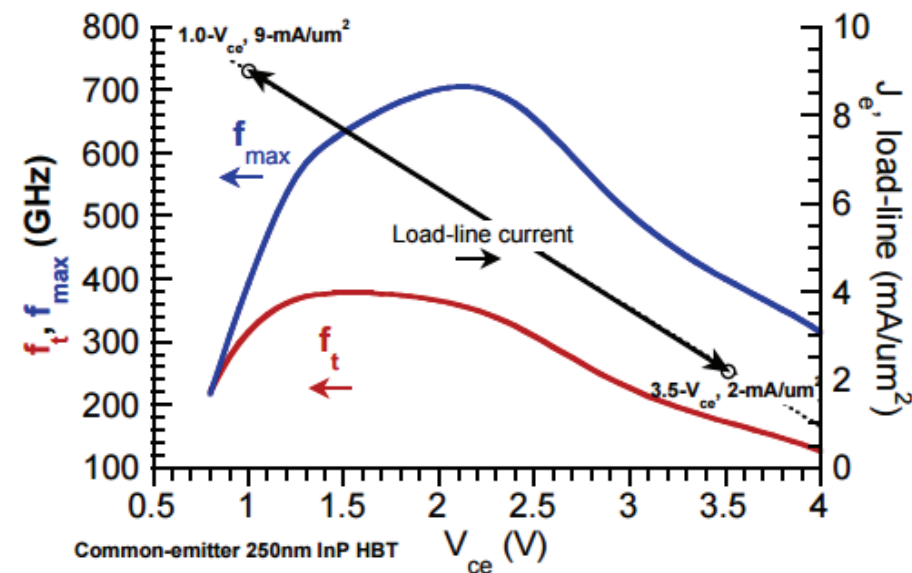
reduction in f_{τ} , increase in C_{cb} → reduced bandwidth

High voltage:

all semiconductors: push-out of collector depletion edge

III-V semiconductors: reduction of electron velocity in collector

reduction in f_{τ} → reduced bandwidth



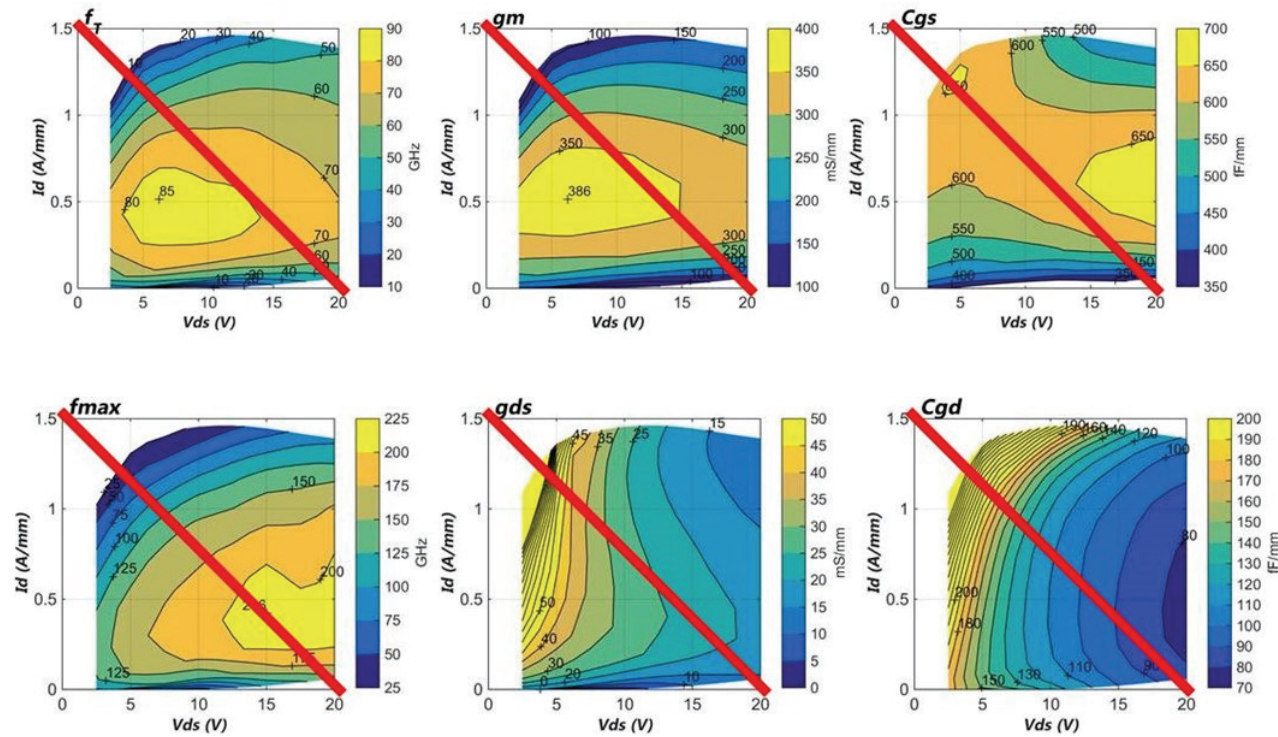
Z. Griffith, 2012 IPRM

Transistor parameters and cutoff frequencies vary across (I,V) plane

Field-Effect Transistors:

Device parameters vary strongly across (I,V) plane

(f_{τ}, f_{\max}) vary strongly across (I,V) plane



GaN HEMT experimental data (c.a. 2010) due to Kiesuke Shinohara, Teledyne Scientific

Safe Operating Area (SOA); "Fast Operating Area" (FOA ?)

Safe operating area

standard terminology

region bounded by maximum power hyperbola, V_{br} , I_{max}

SOA includes other effects beyond the scope of these notes

"Fast operating area"

not standard terminology

region with adequately high f_t , f_{max}

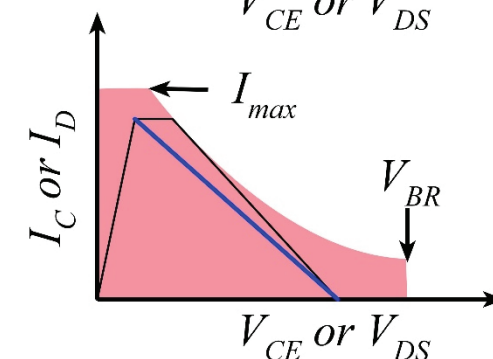
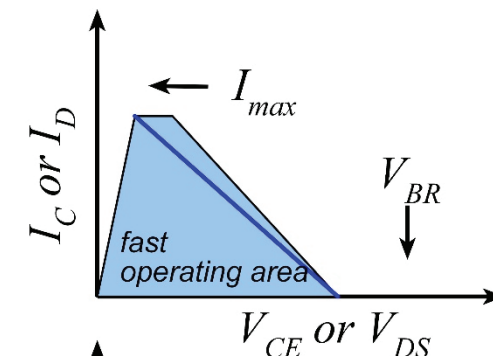
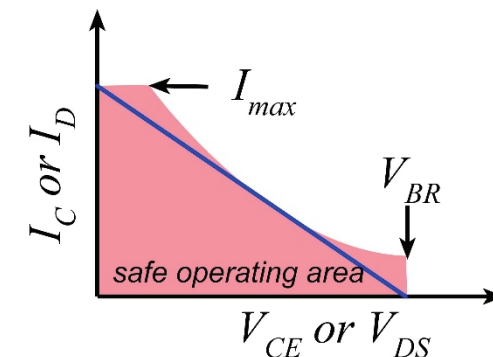
Loadline must lie within both

Reliability

Particularly with Si MOSFETs,

reliability decreases as V_{DS} increases.

→ maximum V_{DS} well below DC breakdown

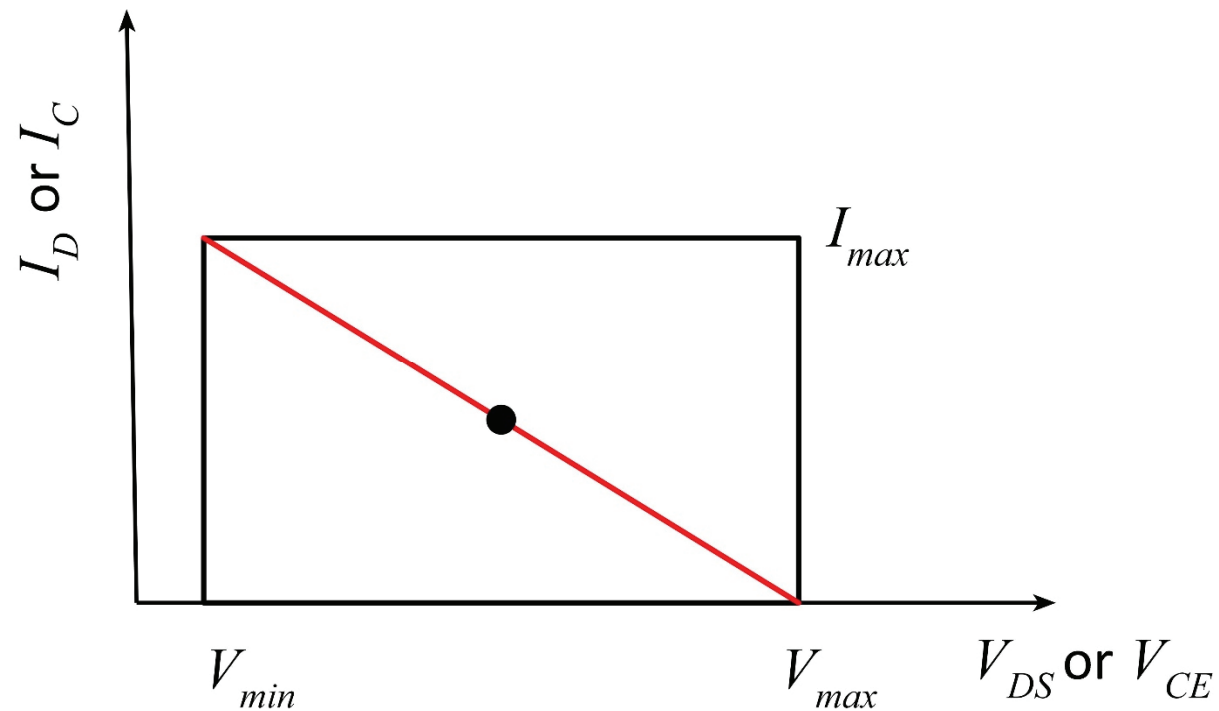


safe operating area
 fast operating area
 loadline

Oversimplified SOA/FOA; for class

Maximum, minimum voltages

Maximum current $\propto N_g W_g$ or $N_E L_E$



Simple class A power analysis

Bias point in center of rectangle.

Loadline reaches corners of rectangle

$$Z_L = R_L + j0\Omega = (V_{\max} - V_{\min}) / I_{\max}$$

$$P_{DC} = V_{DC} I_{DC} = (V_{\max} + V_{\min}) I_{\max} / 4$$

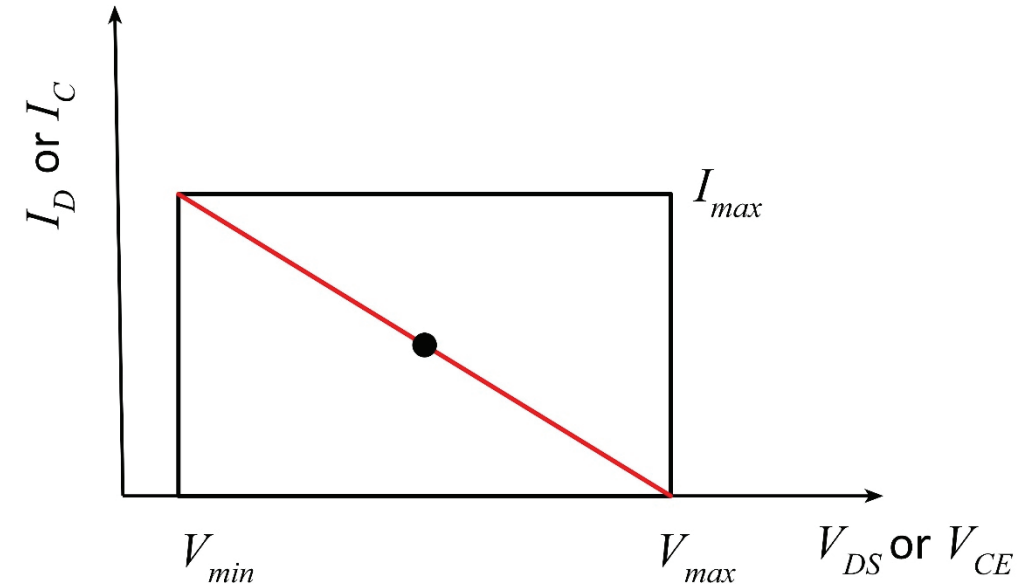
$$P_{RF,\max} = (V_{\max} - V_{\min}) I_{\max} / 8 = (V_{\max} - V_{\min})^2 / 8R_L$$

drain/collector efficiency at peak output power

$$\eta_{\text{drain/collector}} = \frac{P_{RF,\max}}{P_{DC}} = \frac{(V_{\max} - V_{\min}) I_{\max} / 8}{(V_{\max} + V_{\min}) I_{\max} / 4}$$

$$\eta_{\text{drain/collector}} = \frac{1}{2} \frac{V_{\max} - V_{\min}}{V_{\max} + V_{\min}}$$

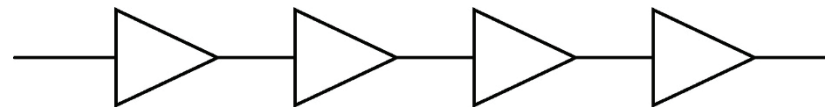
...all expressions correct if and only if $Z_L = (V_{\max} - V_{\min}) / I_{\max}$.



Power-added efficiency

$$\text{P.A.E.} \equiv (P_{out} - P_{in}) / P_{DC}$$

$$= \frac{P_{out}}{P_{DC}} \left[1 - \frac{P_{in}}{P_{out}} \right] = \eta_{\text{drain/collector}} \cdot \left[1 - \frac{1}{\text{gain}} \right] \text{ where } \eta_{\text{drain/collector}} = \frac{P_{out}}{P_{DC}}$$



$$\text{PAE}_{\text{overall}} = \frac{P_{out,N} - P_{in1}}{P_{DC1} + P_{DC2} + \dots + P_{DC,N}} = \frac{(P_{out,N} - P_{in,N}) + (P_{out,N-1} - P_{in,N-1}) + \dots + (P_{out1} - P_{in1})}{P_{DC1} + P_{DC2} + \dots + P_{DC,N}}$$

$$= \frac{1}{P_{DC1} + P_{DC2} + \dots + P_{DC,N}} \left(P_{DC,1} \frac{(P_{out,1} - P_{in,1})}{P_{DC,1}} + P_{DC,2} \frac{(P_{out,2} - P_{in,2})}{P_{DC,2}} \dots + P_{DC,N} \frac{(P_{out,N} - P_{in,N})}{P_{DC,N}} \right)$$

$$= \frac{1}{P_{DC1} + P_{DC2} + \dots + P_{DC,N}} (P_{DC,1} \text{PAE}_1 + P_{DC,2} \text{PAE}_2 + \dots + P_{DC,N} \text{PAE}_N)$$

Now suppose $\text{PAE}_1 = \text{PAE}_2 = \dots = \text{PAE}_N$

$$\text{PAE}_{\text{overall}} = \frac{\text{PAE}_1}{P_{DC1} + P_{DC2} + \dots + P_{DC,N}} (P_{DC,1} + P_{DC,2} + \dots + P_{DC,N}) = \text{PAE}_1$$

A PA chain obtains the same overall PAE as that of 1 stage if

each PA has the same PAE and if each stage in the chain reaches that PAE under the same overall RF drive.

Due to accumulated gain compression, real multistage power amplifiers are rarely designed to meet this criterion.

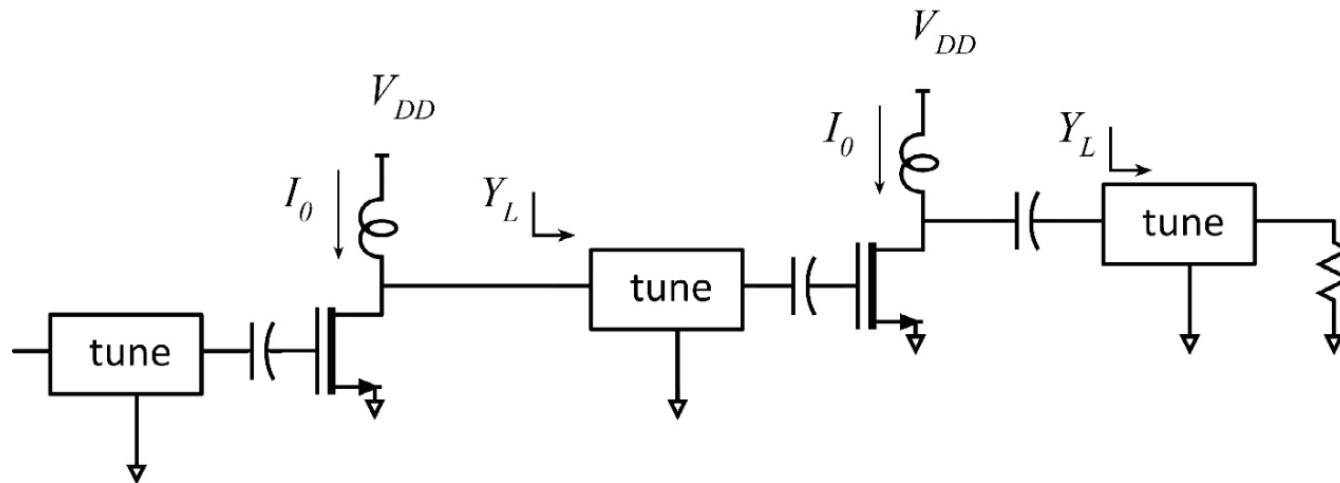
Power Amplifier Design

For highest efficiency, each stage should be loaded with

$$Z_{L,opt} = (V_{\max} - V_{\min}) / I_{\max}$$

The interstage networks are tuning networks,
not matching networks.

Thus far, we have neglected transistor parasitics.



Loadline: inclusive of transistor parasitics

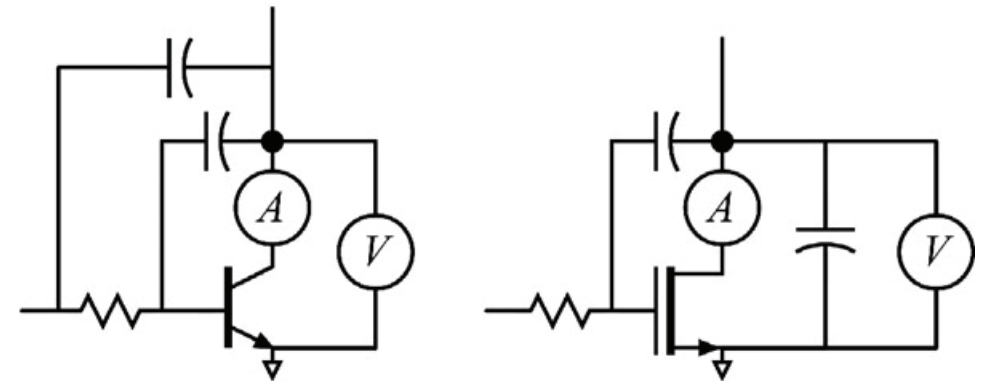
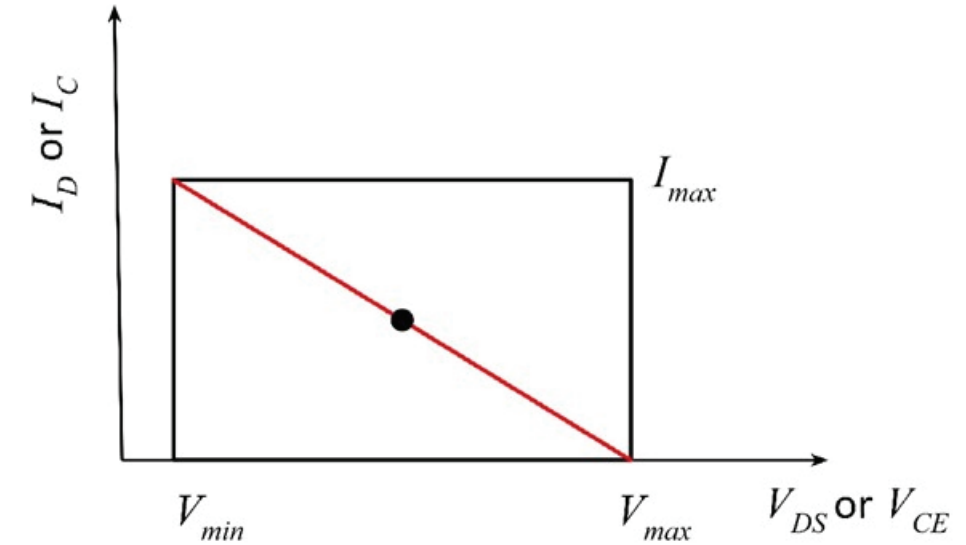
Transistors have resistive, capacitive parasitics.

It is the *internal* (I_C, V_{CE}) or (I_D, V_{DS})
that must follow this loadline \rightarrow

Loadline current must be electron current,
not $C \cdot dV / dt$ displacement current.

\rightarrow Current meters must be placed inside the capacitive parasitics.

How do we do this ?



Loadline inclusive of transistor parasitics

If the transistor technology originates from the organization you work for, then CAD models may not be encrypted.

If so, you can edit the device CAD model to place an internal current meter.

The screenshot shows a schematic editor window titled "scaled_HBT_two [2014_5_DARPA_ACT_lib:scaled_HBT_twoschematic] [Pushed In] (Schematic):2". The interface includes a menu bar (File, Edit, Select, View, Insert, Options, Tools, Layout, Simulate, Window, DynamicLink, DesignGuide, Help) and a toolbar with various icons. On the left, there is a "Parts" panel with a search bar and a list of components under "TLines-Microstrip". The main workspace displays a complex circuit schematic with numerous components labeled with names like "R15", "C1", "R16", "C2", etc. A current meter is placed in series with the collector current path, indicated by an arrow pointing to it. The current meter is labeled "M1" and "M2". The schematic also shows various parasitic elements and connections. The bottom status bar displays "0 items" and "ads_device.drawing -9.875, 11.000 -25.000, 9.375 in".

Loadline inclusive of transistor parasitics

If the transistor technology does not originate from the organization you work for, then the CAD models may be encrypted.

If so

Use design kit CAD device model → simulate device S-parameters

From the S-parameters,

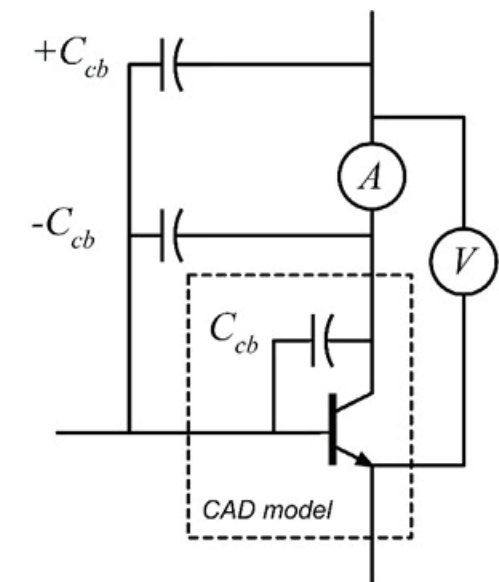
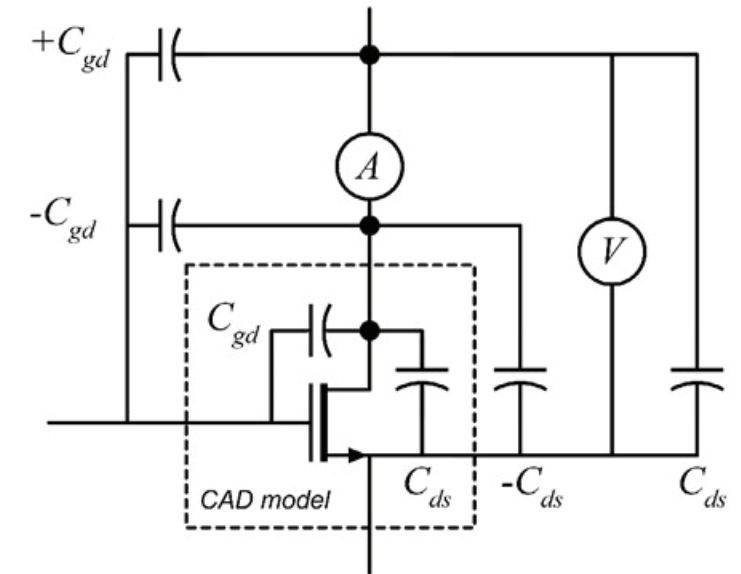
use established extraction procedures to determine transistor capacitances

Then, with transistor capacitances known:

- 1) add external negative capacitances to cancel these.
- 2) add voltmeter and current meter.

These correctly measure the loadline

- 3) then add back external positive capacitances.

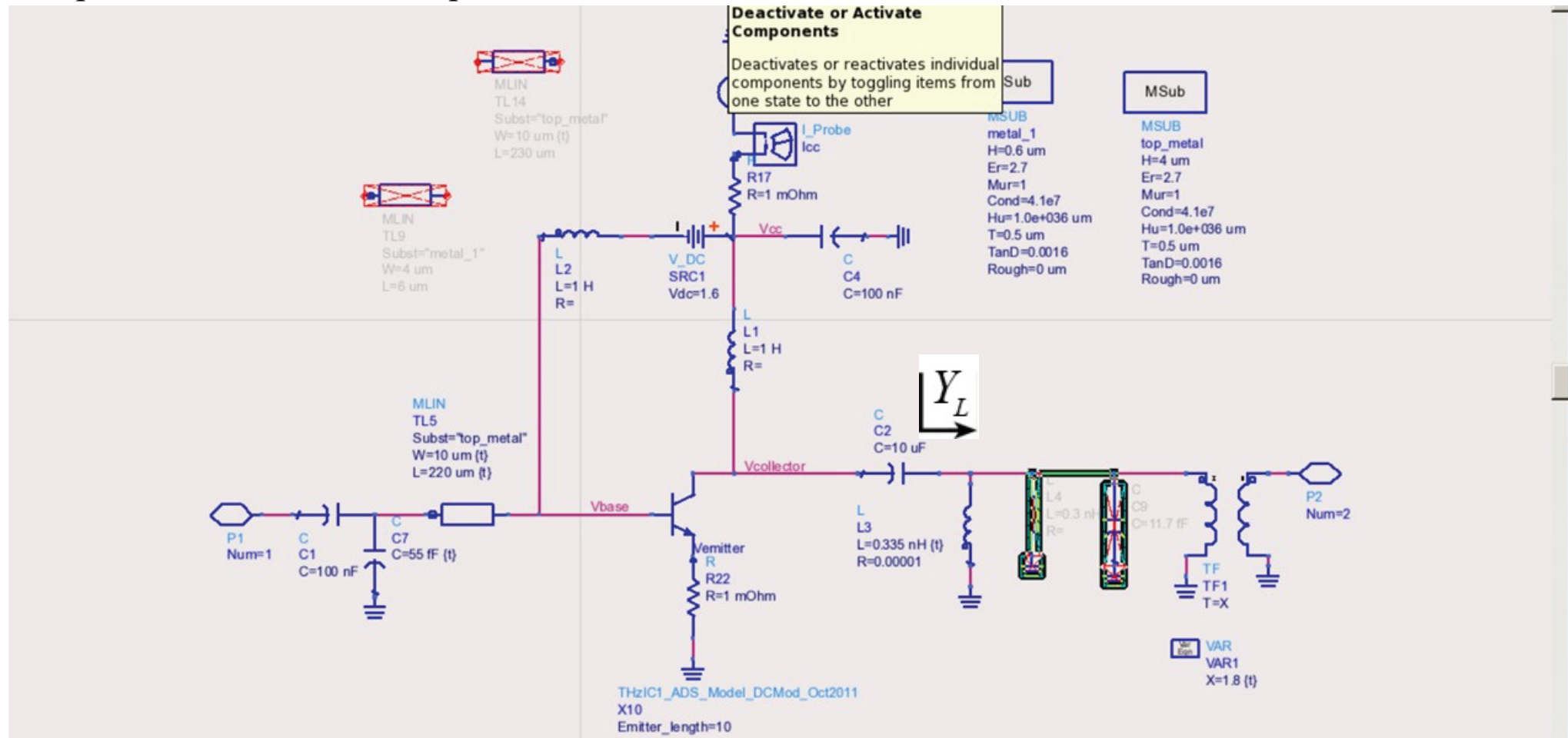


Power Amplifier Design Example

Power amplifier *cell*. 20 micron emitter finger. Bias: $I_c = 10\text{mA}$, $V_{cb} = 1.86\text{ Volts}$ $\rightarrow V_{CE} = 2.5\text{ V}$.

The biasing technique used is just for CAD experimentation; (not practical bias circuit)

The inactivated output LC network is a bandpass filter



Power Amplifier Design Example

First, simulate the transistor S-parameters vs. frequency at the bias point

Determine:

f_{\max} ,

stability factors, stability circles at the design frequency.

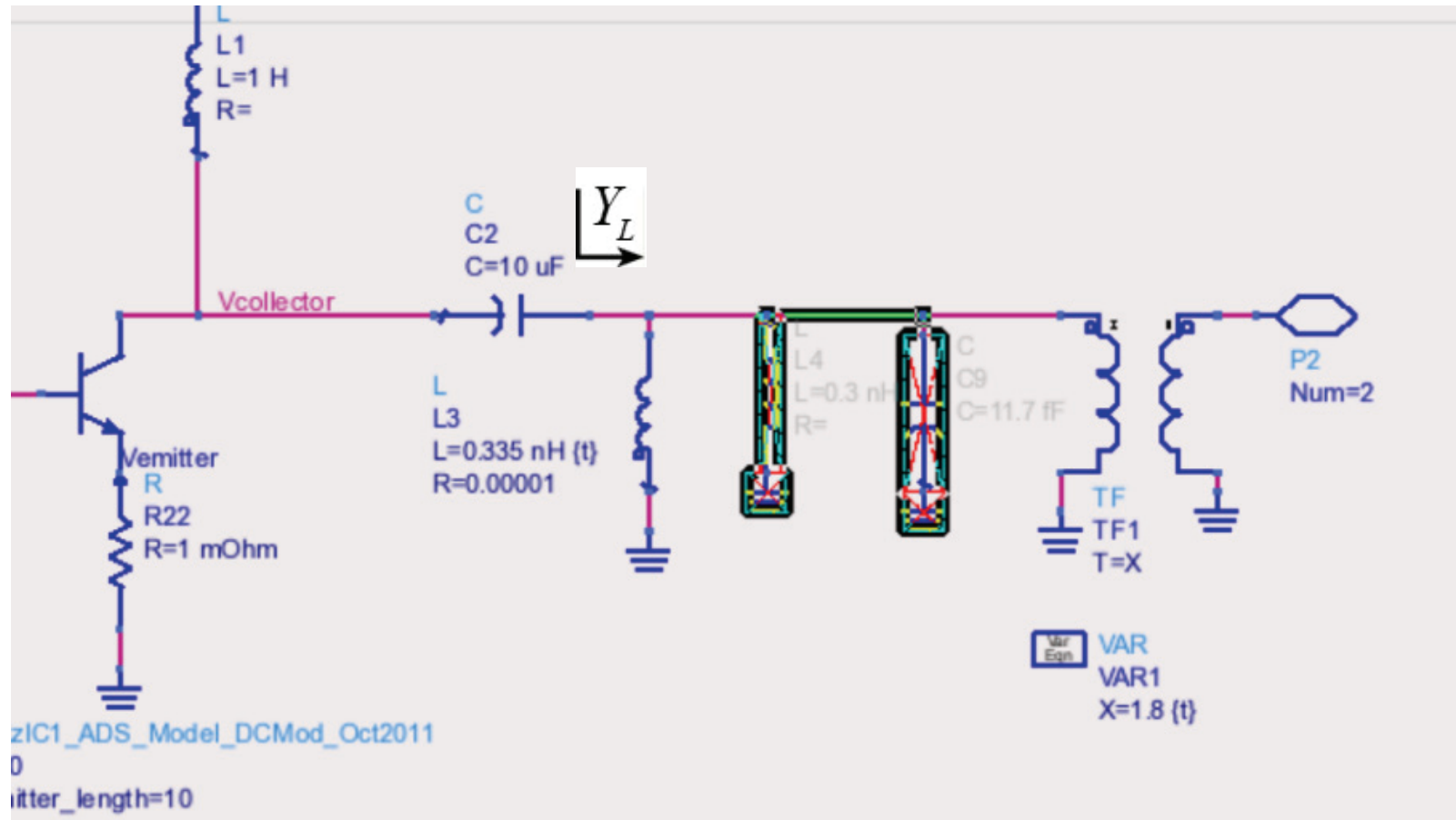
MAG/MSG at the design frequency.

If potentially unstable, stabilize (input resistance or reactive feedback) at the design frequency

PA example: output network

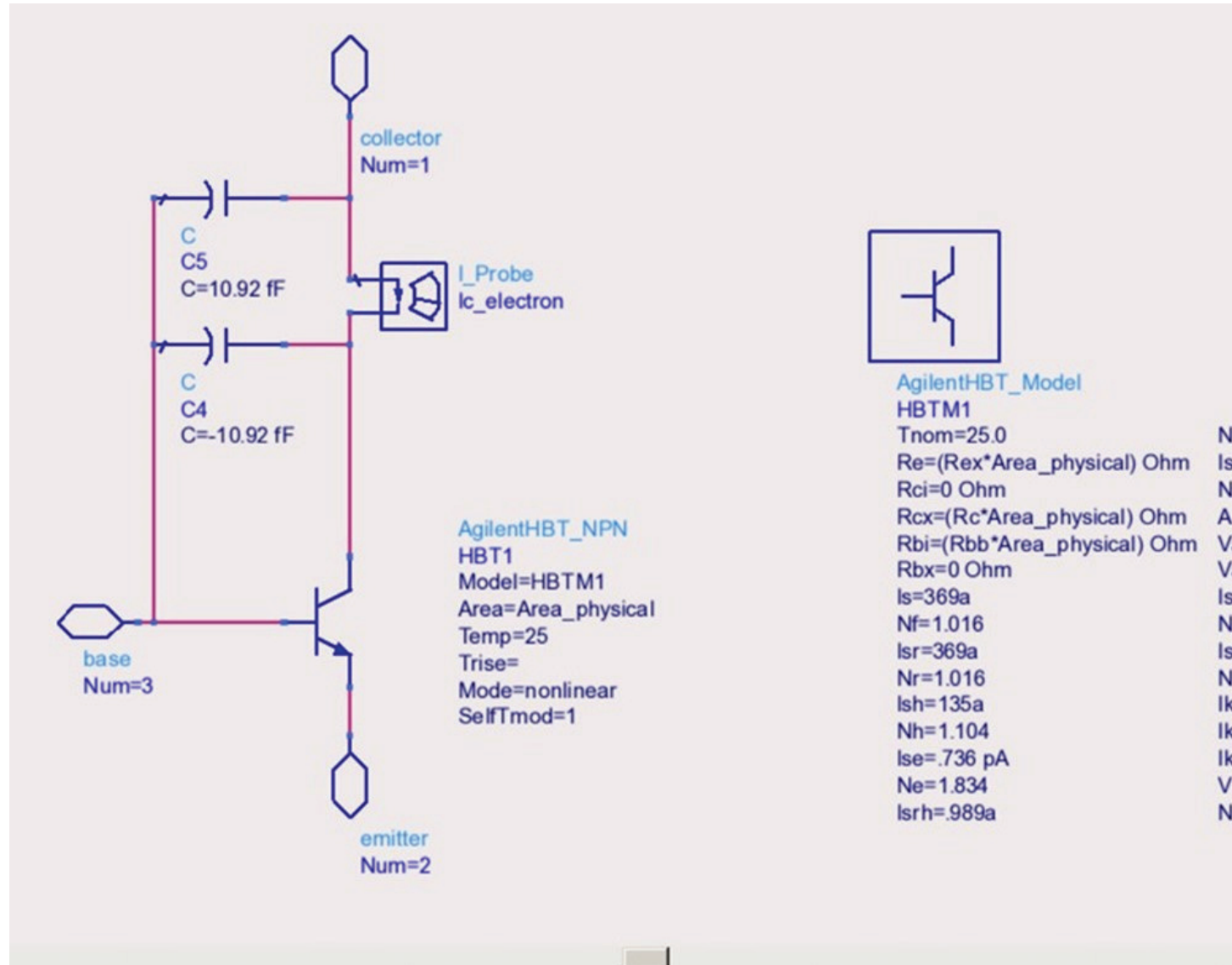
Note the output network: ideal transformer plus parallel inductance.

This is not the final output network: it is used to quickly find $Y_{L,opt}$.



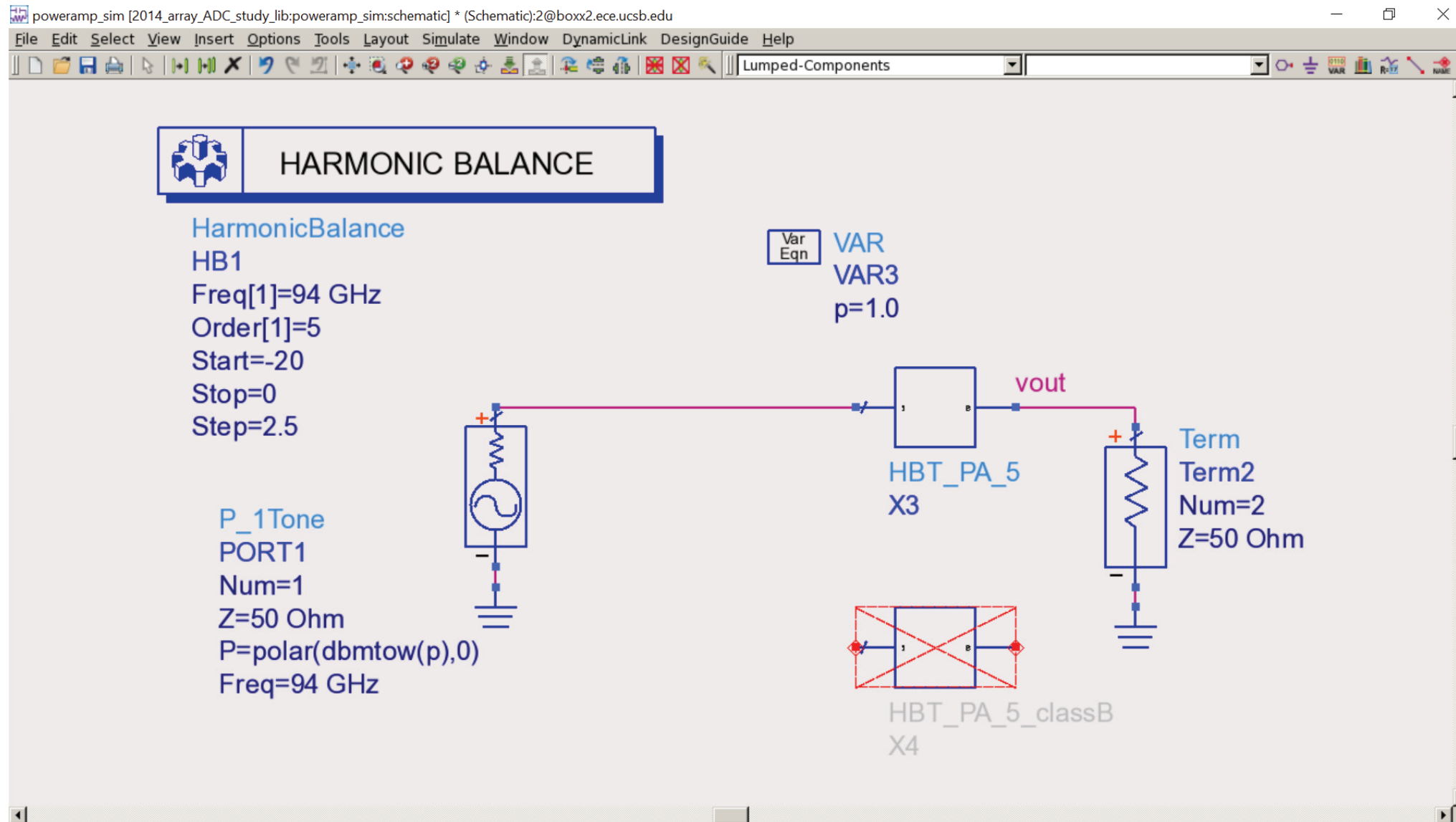
PA example: measuring the loadline

Dropping down in the hierarchy into the device model, we see the monitoring ammeter plus negative and positive C_{cb} .



PA example: finding the optimum load

The input is not yet matched, and the load is not yet tuned. We drive the transistor with a large drive signal and observe the loadline



Lissajous patterns

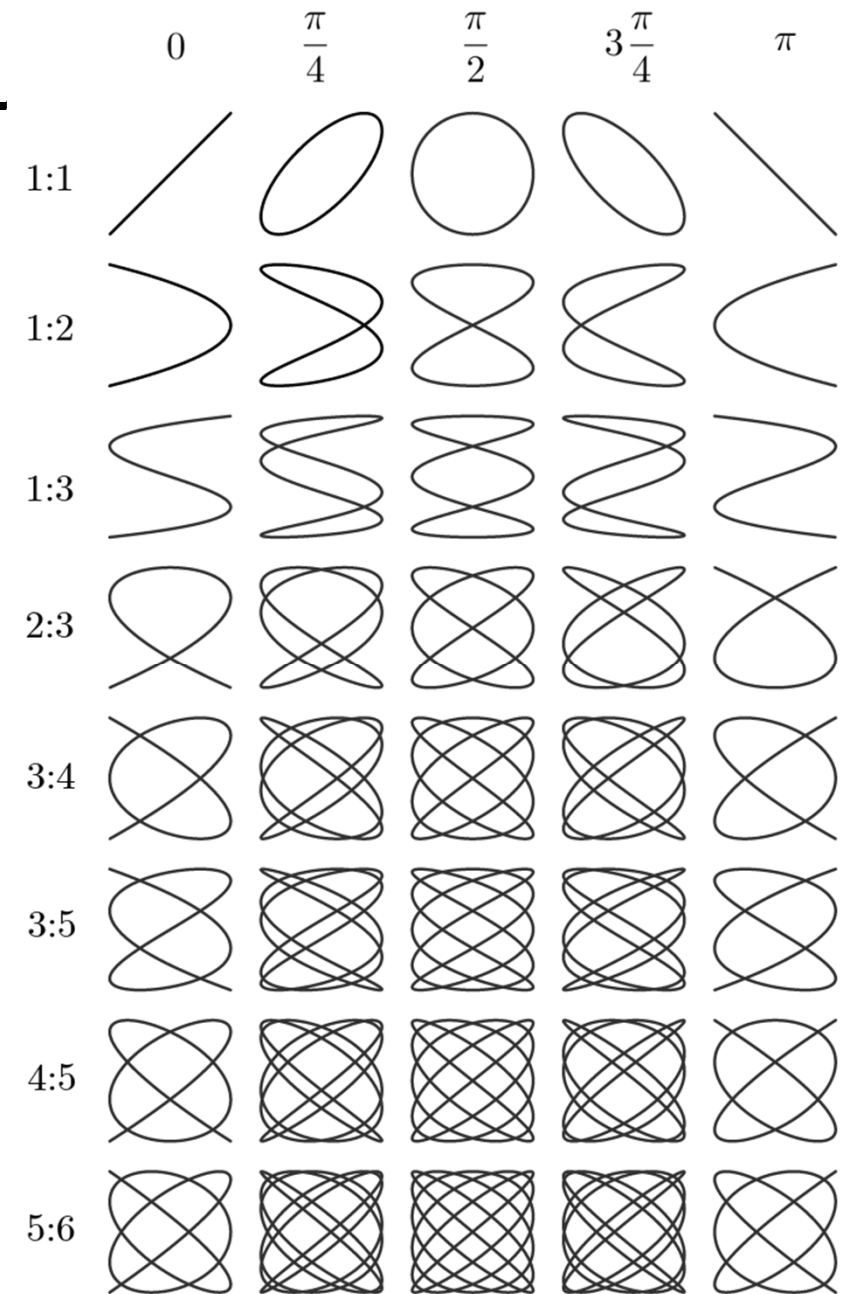
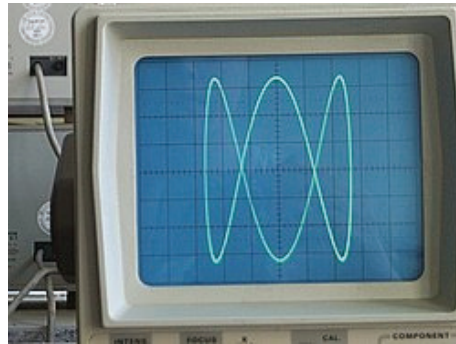
$$x = A \cos(at + \theta)$$

$$y = B \cos(bt)$$

closed patterns if a/b is rational.

a/b or b/a sets # of loops.

for $a=b$, θ varies the curve between a line and an ellipse.



Wikipedia

https://en.wikipedia.org/wiki/Lissajous_curve

Lissajous curve

This article includes a list of general references, but it lacks sufficient corresponding inline citations. (November 2010)

A **Lissajous curve** ⁱ/ˈlɪsəˈʒuː, also known as **Lissajous figure** or **Bowditch curve** ⁱ/ˈboʊdɪttʃ, is the graph of a system of parametric equations

$$x = A \sin(at + \delta), \quad y = B \sin(bt),$$

which describe the superposition of two perpendicular oscillations in x and y directions of different angular frequency (a and b). The resulting family of curves was investigated by Nathaniel Bowditch in 1815, and later in more detail in 1857 by Jules Antoine Lissajous (for whom it has been named). Such motions may be considered as a particular kind of complex harmonic motion.

A Lissajous figure, made by releasing sand from a container at the

https://en.wikipedia.org/wiki/Lissajous_curve

https://en.wikipedia.org/wiki/Lissajous_curve#/media/File:Lissajous_relaciones.png

Reactive load: I vs. V is ellipse in (V,I) plane.

$$V_{DS}(t) = V_{DC} + V_{peak} \cos(\omega t + \theta)$$

$$I_{D,internal}(t) = I_{DC} + I_{peak} \cos(\omega t)$$

$\theta = 0^\circ$ or 180°

→ $I_{D,internal}$ vs. $V_{DS,internal}$ is **straight line in (V, I) plane**

$$\rightarrow Y_{L,internal} = (I_{peak} / V_{peak}) \exp(-j\theta) = G_{L,internal} + jB_{L,internal}$$

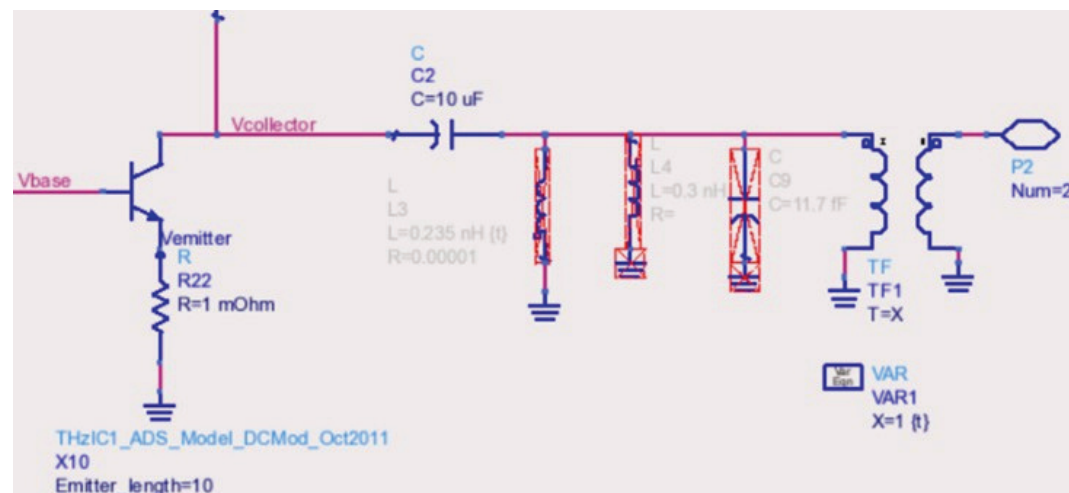
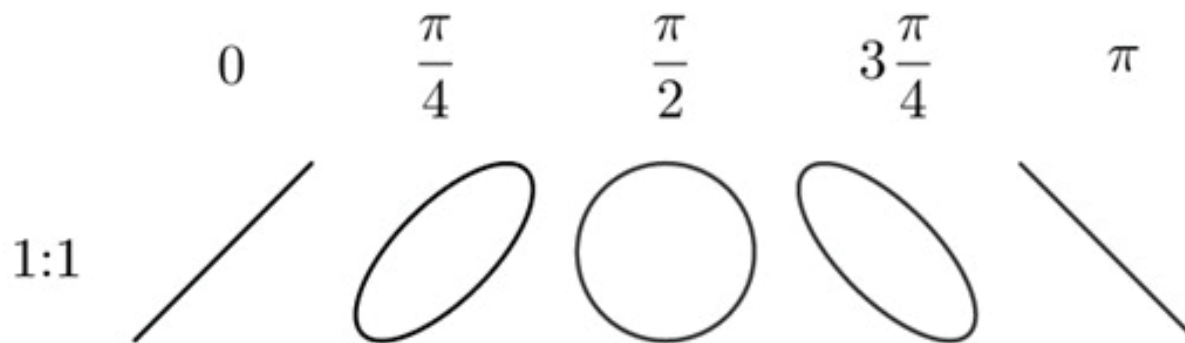
$Y_{L,internal} = G_{L,internal} + j0 \text{ S}$ is purely real admittance.

$\theta \neq 0^\circ$ and $\neq 180^\circ$

→ I_D vs. V_{DS} is **ellipse in (V, I) plane**

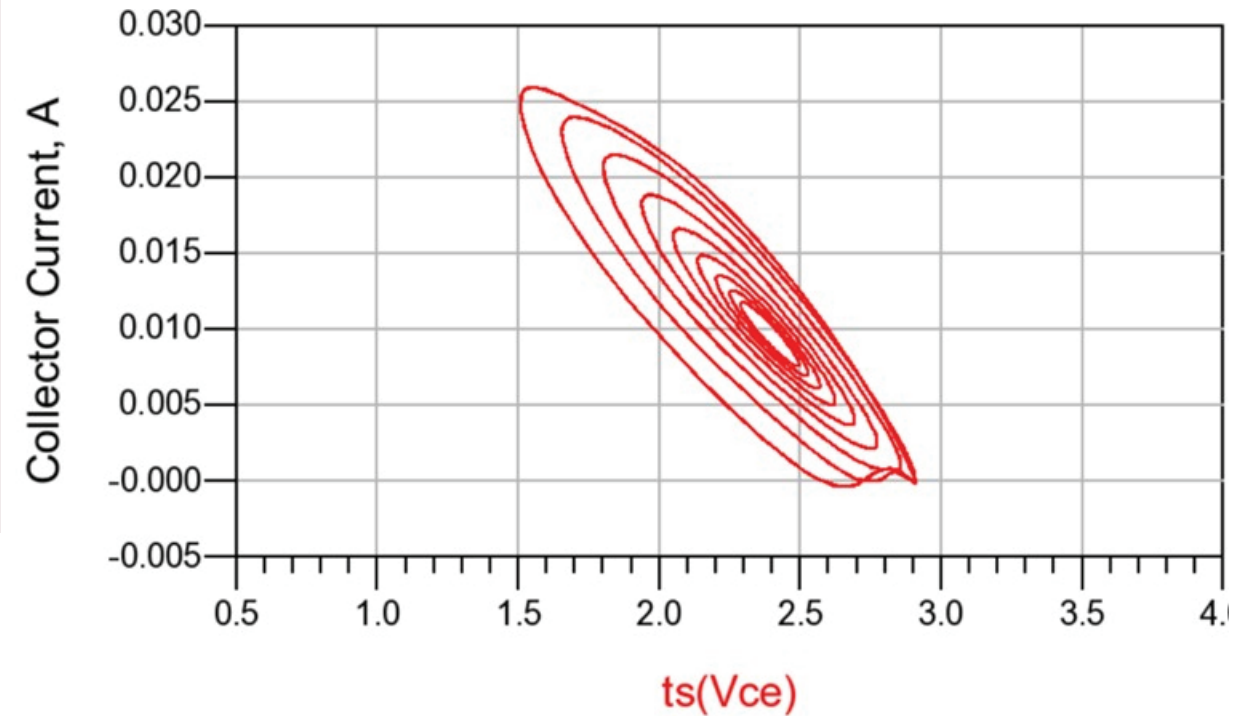
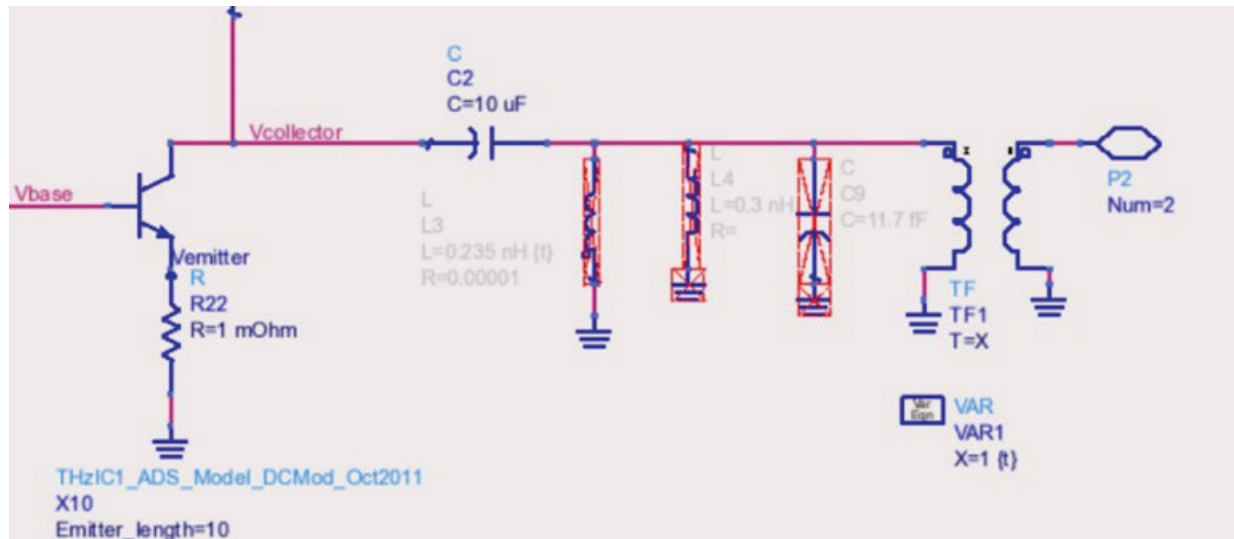
$$\rightarrow Y_{L,internal} = (I_{peak} / V_{peak}) \exp(-j\theta)$$

$Y_{L,internal} = G_{L,internal} + jB_{L,internal}$ with $B_{L,internal} \neq 0 \text{ S}$; nonzero load susceptance



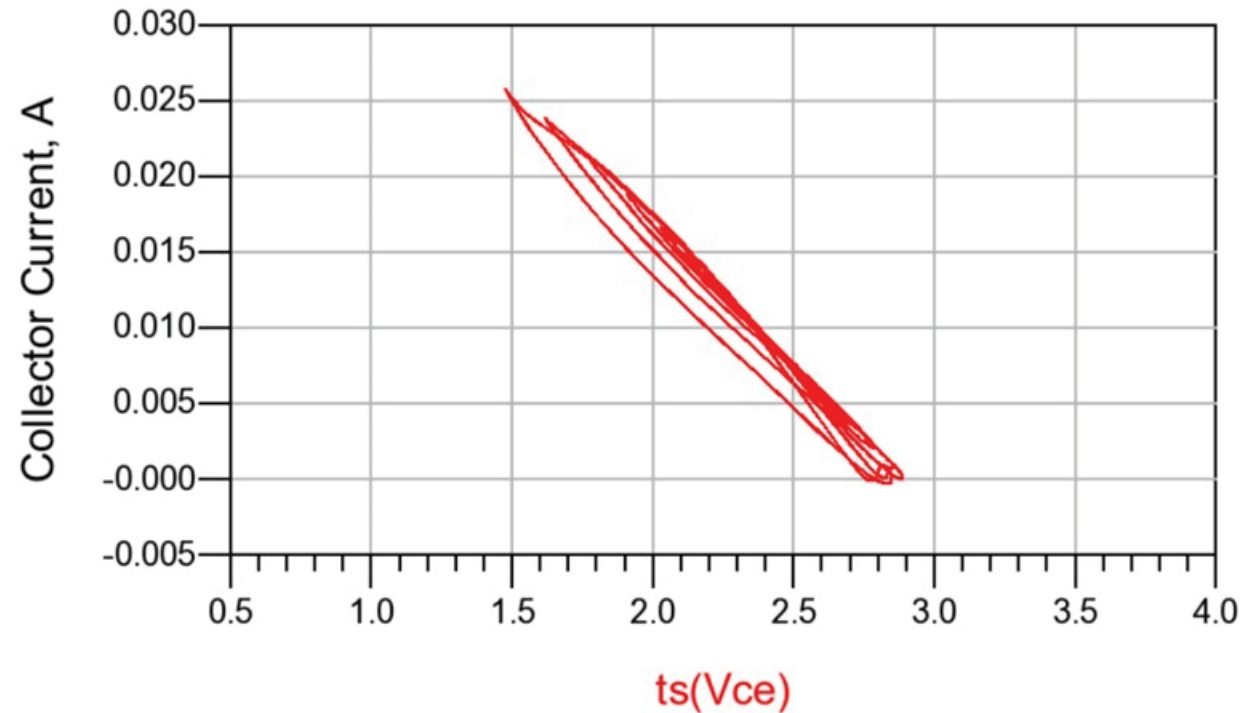
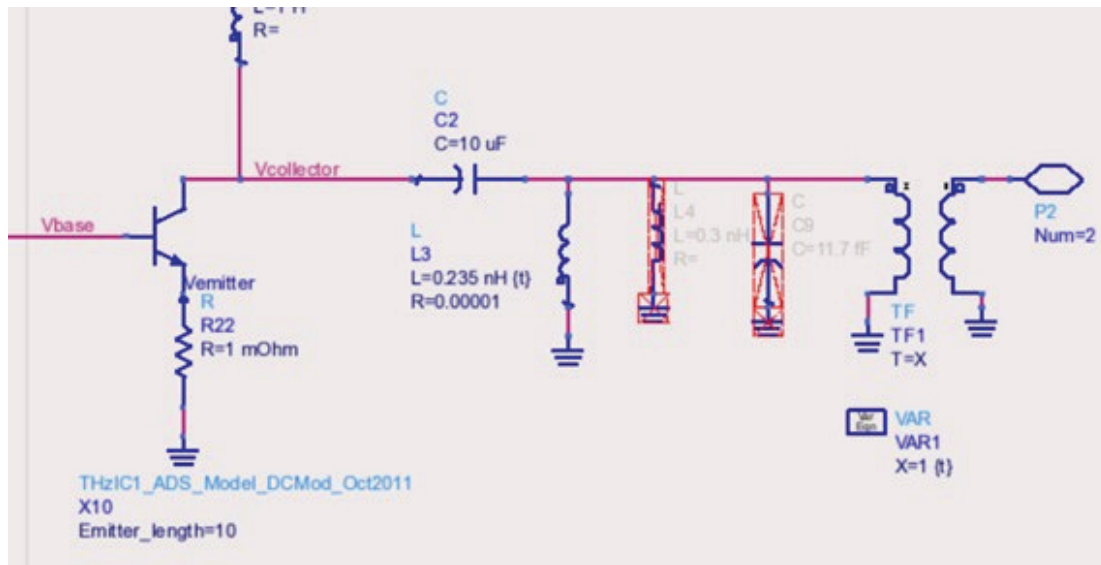
Power Amplifier Design Example

With no inductive tuning, and with a 1:1 transformer ratio, the loadline initially looks like this:



Power Amplifier Design Example

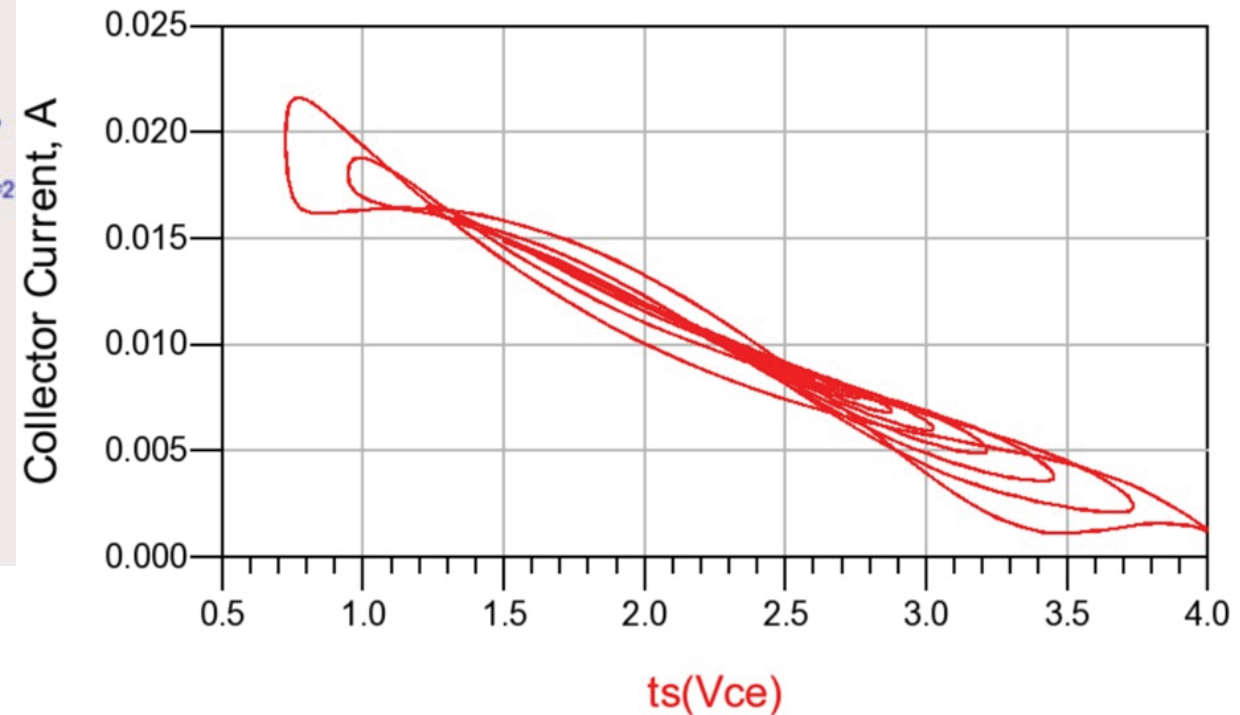
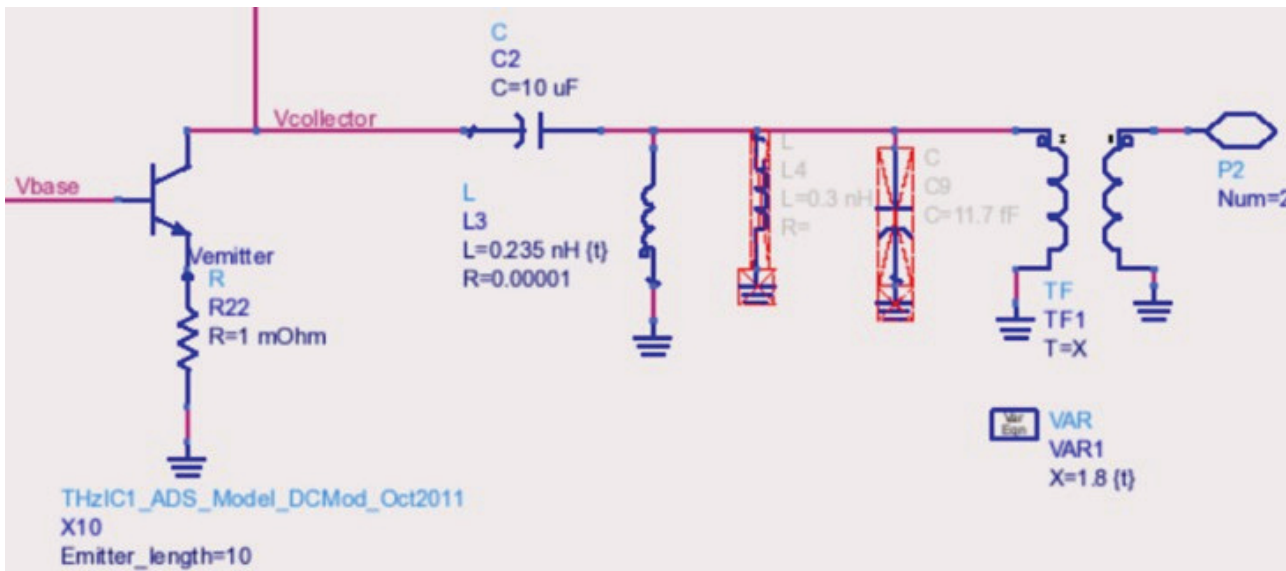
First add the inductive tuning, adjusting the shunt inductance, L , to eliminate loadline looping



Power Amplifier Design Example

Then adjust the transformer ratio to obtain a loadline passing through the target endpoints (V_{\min}, I_{\max}) and ($V_{\max}, I_{\min} = 0A$)

We had expected a straight line. The looping (3 per cycle) is 3rd harmonic generation (consider again the Lissajous patterns)

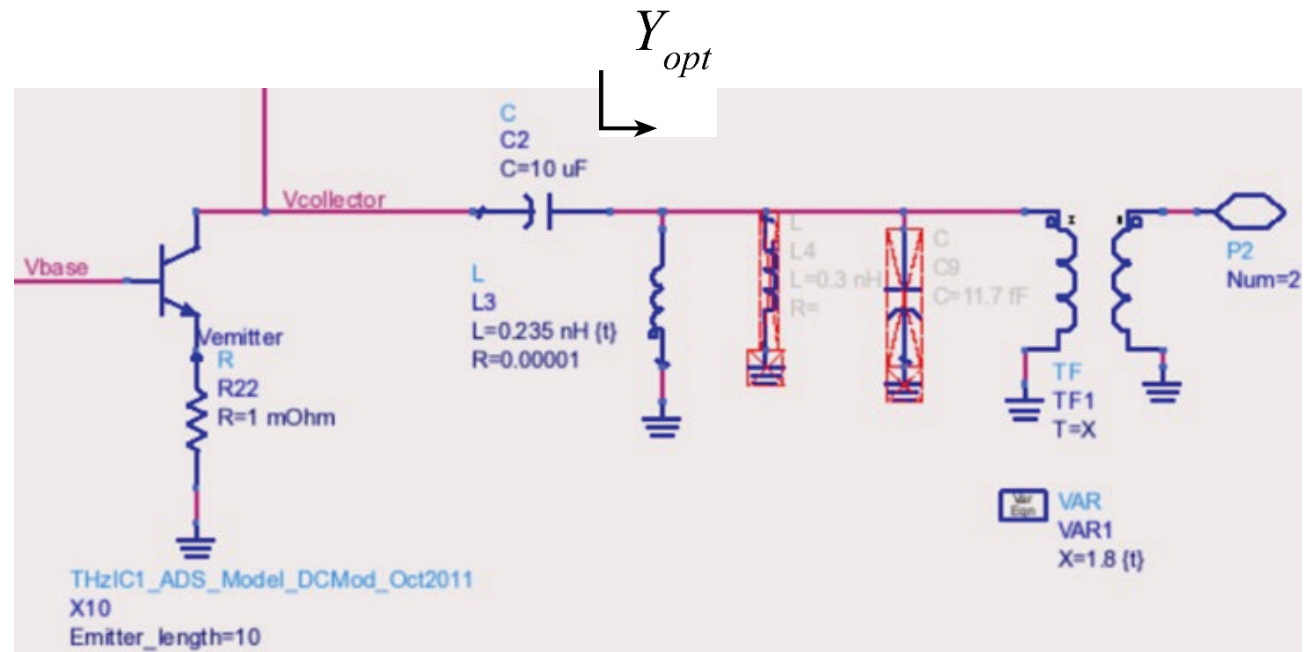


Power Amplifier Design Example

We have now determined Y_{opt} .

In this example:

$$\begin{aligned}
 Y_{opt} &= \frac{1}{j\omega L} + \left(\frac{1}{\text{transformer turns ratio}} \right)^2 \frac{1}{50\Omega} \\
 &= \frac{1}{j\omega L} + \left(\frac{1}{X} \right)^2 \frac{1}{50\Omega} \\
 &= \frac{1}{j \cdot 2\pi \cdot 94 \text{ GHz} \cdot 0.235 \text{ nH}} + \left(\frac{1}{1.8} \right)^2 \frac{1}{50\Omega}
 \end{aligned}$$

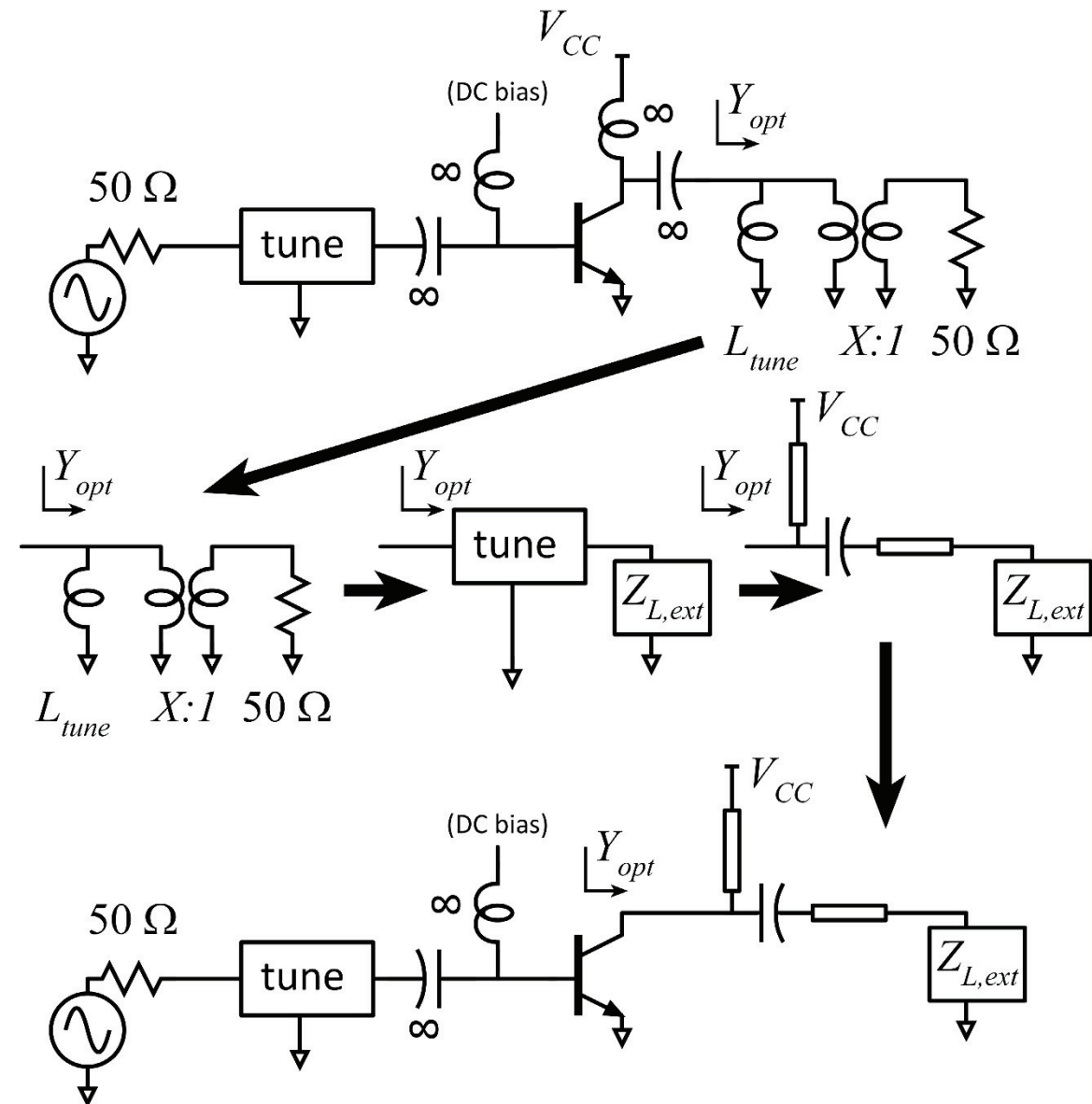


Power Amplifier Design Example

With Y_{opt} now determined,

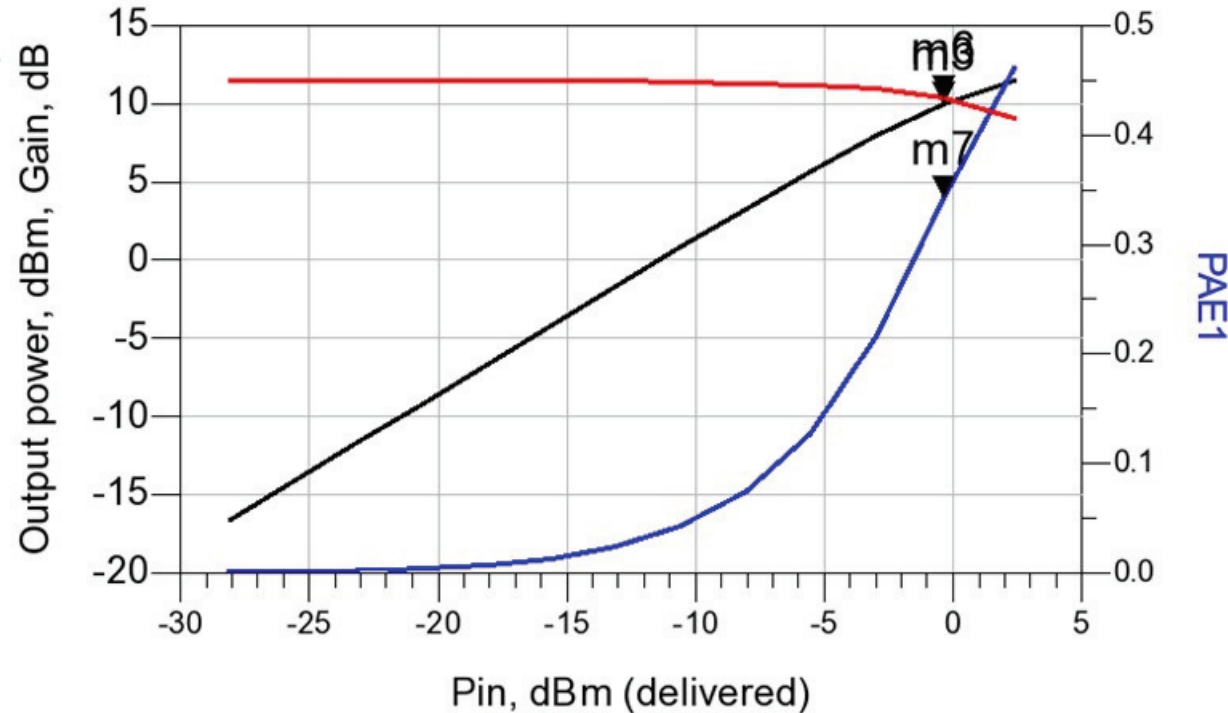
We then design a practical output network which that provides this Y_{opt} .

We then add this to the PA.



Power Amplifier Design Example

Here is our final simulated performance



Other issues:

Input matching network

Out-of-band stabilization

(ece145a)

Often: filters

to suppress 2nd, 3rd harmonics.

```
m6
indep(m6)=-0.394
plot_vs(pout-Pin_deliv_dBm, Pin_deliv_dBm)=10.379
```

```
m7
indep(m7)=-0.394
plot_vs(PAE1, Pin_deliv_dBm)=0.342
```

```
m3
indep(m3)=-0.394
plot_vs(pout, Pin_deliv_dBm)=9.985
```

Load pull method

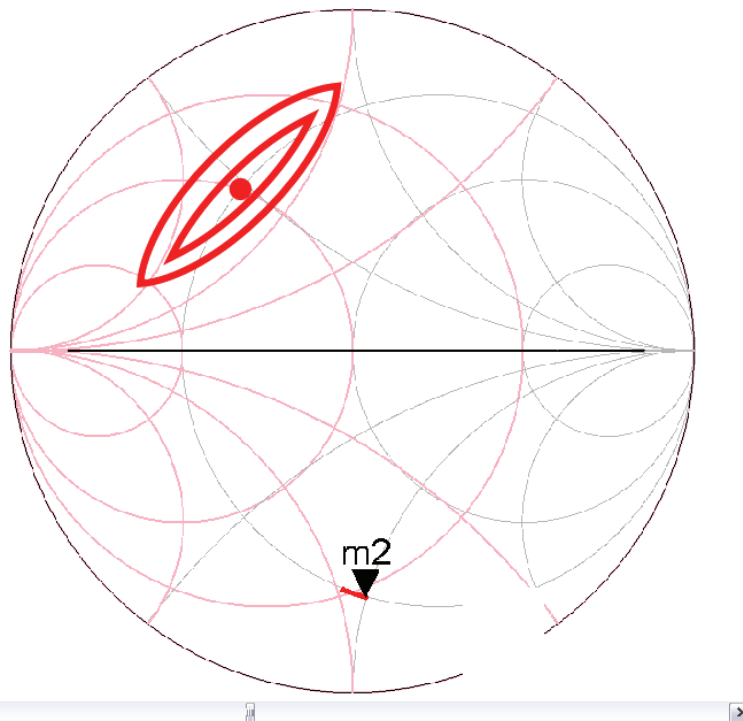
We can also empirically determine (in CAD, or with instruments) the load impedance giving the largest saturated P_{out} .

We then use this impedance for our PA design

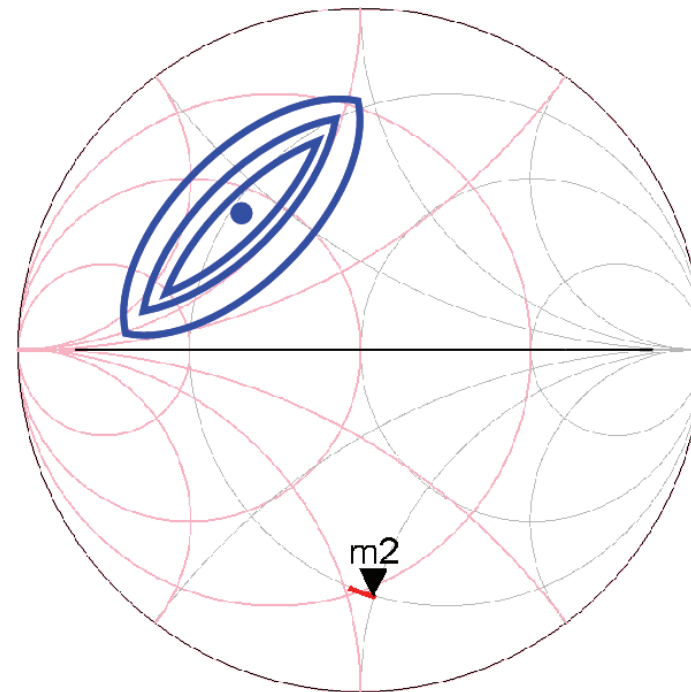
Empirical method. Simply contour plots of maximum P_{out} and peak PAE

Steven Cripps has a paper that shows that these contours are sets of intersecting ellipses on the Smith chart.

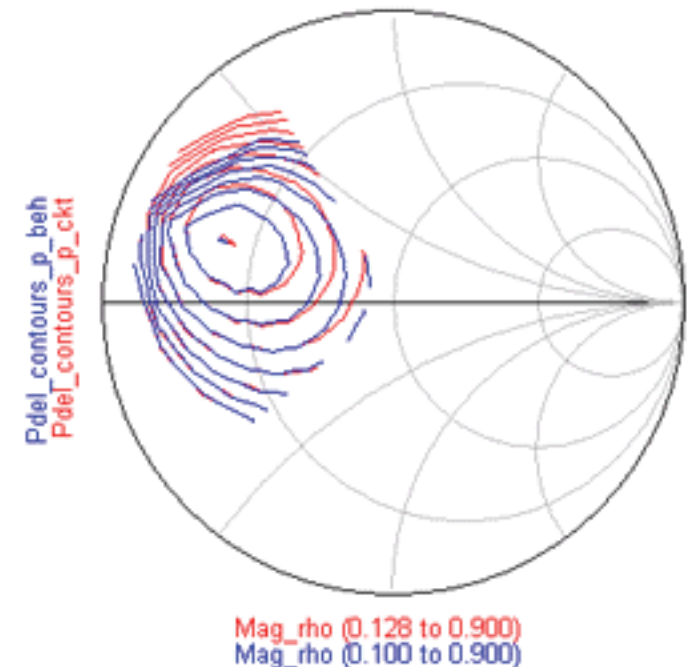
P_{sat} contours



PAE contours



Keysight ADS plot



Load pull method

We can also empirically determine (in CAD, or with instruments) the load impedance giving the largest saturated P_{out} . We then use this impedance for our PA design. Keysight ADS and other CAD packages have pre-configured test benches to do this.

System Reference Impedance
60.000

PAE (thick) and Delivered Power (thin) Contours

Set Delivered Power contour step size (dB) and PAE contour step size (%), and number of contour lines

- Eqn PdEl_step=0.5
- Eqn PAE_step=4
- Eqn NumPAE_lines=5
- Eqn NumPdEl_lines=5

Maximum Power-Added Efficiency, %
40.8%

Maximum Power Delivered, dBm
25.67

Indep:PAE_contour_p1: 0.000 to 32.000
Indep:PAE_contour_p2: 0.000 to 41.000

Re-Normalized PAE (thick) and Delivered Power (thin) Contours

Set new reference impedance:
Eqn ZDnew=10

Two Tone Load Pull Simulation; output power, PAE, 3rd- and 5th-Order Intermodulation Distortion levels found at each fundamental load impedance

Specify desired Fundamental Load Tuner coverage:
s11_rho is the radius of the circle of reflection coefficients simulated. However, the radius of the circle will be reduced if it would otherwise go outside the Smith chart. If you want to override this and allow reflection coefficients outside the Smith chart, edit the SweepEquations VAR block, and set max_rho=mag(s11_rho)
s11_center is the center of the circle of simulated reflection coefficients
pts is total number of reflection coefficients simulated
Z0 is the system reference impedance

VAR SweepEquations
s11_rho = 0.75
s11_center = 0.6 + j0.2
pts=100
Z0=50

Equations are on the "Equations" page.

Move Marker m3 to select impedance value and corresponding PAE and delivered power values.

Impedance at marker m3
6.995 + j7.849

PAE, %
31.28

Power Delivered (dBm)
25.19

Set these values:
VAR STIMULUS
Pavs=10_dBm
RFfreq=850 MHz
fspacing=50 kHz
Max_IMD_order=7
Vhigh=5.8
Vlow=2

PARAMETER SWEEP
Sweep1

HARMONIC BALANCE
Harmonic balance
HB1
MaxOrder=Max_IMD_order
Freq[1]=RFfreq+fspacing/2
Freq[2]=RFfreq+fspacing/2
Order[1]=7
Order[2]=7
UseKrylov=yes
Other

VAR VAR1
cells=28

Set Load and Source impedances at baseband and harmonic frequencies

VAR VAR2
Z_j_bb = 1000 + j0
Z_j_2 = 1000 + j0
Z_j_3 = 1000 + j0
Z_j_4 = 1000 + j0
Z_j_5 = 1000 + j0
Z_s_bb = 1000 + j0
Z_s_fund = 10 + j0
Z_s_2 = 1000 + j0
Z_s_3 = 1000 + j0
Z_s_4 = 1000 + j0
Z_s_5 = 1000 + j0

Refer to the PowerPoint (TM) presentation "LoadPullPres ppt" within this example project directory for a detailed explanation of these load pull simulation setups.

VAR global ImpedanceEquations

hpmos
File="motorola_mosfet_h"

Simulated Load Reflection Coefficients

max_imag[11] (-0.966 to -0.234)

max_real[11] (-0.722 to 0.181)

max_imag[12] (-0.722 to 0.181)

max_real[12] (-0.234 to 0.966)

max_imag[13] (-0.234 to 0.966)

max_real[13] (-0.966 to -0.722)

max_imag[14] (-0.234 to 0.966)

max_real[14] (-0.722 to 0.181)

max_imag[15] (-0.722 to 0.181)

max_real[15] (-0.234 to 0.966)

max_imag[16] (-0.966 to -0.722)

max_real[16] (-0.722 to 0.181)

max_imag[17] (-0.722 to 0.181)

max_real[17] (-0.234 to 0.966)

max_imag[18] (-0.234 to 0.966)

max_real[18] (-0.966 to -0.722)

max_imag[19] (-0.722 to 0.181)

max_real[19] (-0.234 to 0.966)

max_imag[20] (-0.966 to -0.722)

max_real[20] (-0.722 to 0.181)

max_imag[21] (-0.722 to 0.181)

max_real[21] (-0.234 to 0.966)

max_imag[22] (-0.234 to 0.966)

max_real[22] (-0.966 to -0.722)

max_imag[23] (-0.722 to 0.181)

max_real[23] (-0.234 to 0.966)

max_imag[24] (-0.966 to -0.722)

max_real[24] (-0.722 to 0.181)

max_imag[25] (-0.722 to 0.181)

max_real[25] (-0.234 to 0.966)

max_imag[26] (-0.234 to 0.966)

max_real[26] (-0.966 to -0.722)

max_imag[27] (-0.722 to 0.181)

max_real[27] (-0.234 to 0.966)

max_imag[28] (-0.966 to -0.722)

max_real[28] (-0.722 to 0.181)

max_imag[29] (-0.722 to 0.181)

max_real[29] (-0.234 to 0.966)

max_imag[30] (-0.234 to 0.966)

max_real[30] (-0.966 to -0.722)

max_imag[31] (-0.722 to 0.181)

max_real[31] (-0.234 to 0.966)

max_imag[32] (-0.966 to -0.722)

max_real[32] (-0.722 to 0.181)

max_imag[33] (-0.722 to 0.181)

max_real[33] (-0.234 to 0.966)

max_imag[34] (-0.234 to 0.966)

max_real[34] (-0.966 to -0.722)

max_imag[35] (-0.722 to 0.181)

max_real[35] (-0.234 to 0.966)

max_imag[36] (-0.966 to -0.722)

max_real[36] (-0.722 to 0.181)

max_imag[37] (-0.722 to 0.181)

max_real[37] (-0.234 to 0.966)

max_imag[38] (-0.234 to 0.966)

max_real[38] (-0.966 to -0.722)

max_imag[39] (-0.722 to 0.181)

max_real[39] (-0.234 to 0.966)

max_imag[40] (-0.966 to -0.722)

max_real[40] (-0.722 to 0.181)

max_imag[41] (-0.722 to 0.181)

max_real[41] (-0.234 to 0.966)

max_imag[42] (-0.234 to 0.966)

max_real[42] (-0.966 to -0.722)

max_imag[43] (-0.722 to 0.181)

max_real[43] (-0.234 to 0.966)

max_imag[44] (-0.966 to -0.722)

max_real[44] (-0.722 to 0.181)

max_imag[45] (-0.722 to 0.181)

max_real[45] (-0.234 to 0.966)

max_imag[46] (-0.234 to 0.966)

max_real[46] (-0.966 to -0.722)

max_imag[47] (-0.722 to 0.181)

max_real[47] (-0.234 to 0.966)

max_imag[48] (-0.966 to -0.722)

max_real[48] (-0.722 to 0.181)

max_imag[49] (-0.722 to 0.181)

max_real[49] (-0.234 to 0.966)

max_imag[50] (-0.234 to 0.966)

max_real[50] (-0.966 to -0.722)

max_imag[51] (-0.722 to 0.181)

max_real[51] (-0.234 to 0.966)

max_imag[52] (-0.966 to -0.722)

max_real[52] (-0.722 to 0.181)

max_imag[53] (-0.722 to 0.181)

max_real[53] (-0.234 to 0.966)

max_imag[54] (-0.234 to 0.966)

max_real[54] (-0.966 to -0.722)

max_imag[55] (-0.722 to 0.181)

max_real[55] (-0.234 to 0.966)

max_imag[56] (-0.966 to -0.722)

max_real[56] (-0.722 to 0.181)

max_imag[57] (-0.722 to 0.181)

max_real[57] (-0.234 to 0.966)

max_imag[58] (-0.234 to 0.966)

max_real[58] (-0.966 to -0.722)

max_imag[59] (-0.722 to 0.181)

max_real[59] (-0.234 to 0.966)

max_imag[60] (-0.966 to -0.722)

max_real[60] (-0.722 to 0.181)

max_imag[61] (-0.722 to 0.181)

max_real[61] (-0.234 to 0.966)

max_imag[62] (-0.234 to 0.966)

max_real[62] (-0.966 to -0.722)

max_imag[63] (-0.722 to 0.181)

max_real[63] (-0.234 to 0.966)

max_imag[64] (-0.966 to -0.722)

max_real[64] (-0.722 to 0.181)

max_imag[65] (-0.722 to 0.181)

max_real[65] (-0.234 to 0.966)

max_imag[66] (-0.234 to 0.966)

max_real[66] (-0.966 to -0.722)

max_imag[67] (-0.722 to 0.181)

max_real[67] (-0.234 to 0.966)

max_imag[68] (-0.966 to -0.722)

max_real[68] (-0.722 to 0.181)

max_imag[69] (-0.722 to 0.181)

max_real[69] (-0.234 to 0.966)

max_imag[70] (-0.234 to 0.966)

max_real[70] (-0.966 to -0.722)

max_imag[71] (-0.722 to 0.181)

max_real[71] (-0.234 to 0.966)

max_imag[72] (-0.966 to -0.722)

max_real[72] (-0.722 to 0.181)

max_imag[73] (-0.722 to 0.181)

max_real[73] (-0.234 to 0.966)

max_imag[74] (-0.234 to 0.966)

max_real[74] (-0.966 to -0.722)

max_imag[75] (-0.722 to 0.181)

max_real[75] (-0.234 to 0.966)

max_imag[76] (-0.966 to -0.722)

max_real[76] (-0.722 to 0.181)

max_imag[77] (-0.722 to 0.181)

max_real[77] (-0.234 to 0.966)

max_imag[78] (-0.234 to 0.966)

max_real[78] (-0.966 to -0.722)

max_imag[79] (-0.722 to 0.181)

max_real[79] (-0.234 to 0.966)

max_imag[80] (-0.966 to -0.722)

max_real[80] (-0.722 to 0.181)

max_imag[81] (-0.722 to 0.181)

max_real[81] (-0.234 to 0.966)

max_imag[82] (-0.234 to 0.966)

max_real[82] (-0.966 to -0.722)

max_imag[83] (-0.722 to 0.181)

max_real[83] (-0.234 to 0.966)

max_imag[84] (-0.966 to -0.722)

max_real[84] (-0.722 to 0.181)

max_imag[85] (-0.722 to 0.181)

max_real[85] (-0.234 to 0.966)

max_imag[86] (-0.234 to 0.966)

max_real[86] (-0.966 to -0.722)

max_imag[87] (-0.722 to 0.181)

max_real[87] (-0.234 to 0.966)

max_imag[88] (-0.966 to -0.722)

max_real[88] (-0.722 to 0.181)

max_imag[89] (-0.722 to 0.181)

max_real[89] (-0.234 to 0.966)

max_imag[90] (-0.234 to 0.966)

max_real[90] (-0.966 to -0.722)

max_imag[91] (-0.722 to 0.181)

max_real[91] (-0.234 to 0.966)

max_imag[92] (-0.966 to -0.722)

max_real[92] (-0.722 to 0.181)

max_imag[93] (-0.722 to 0.181)

max_real[93] (-0.234 to 0.966)

max_imag[94] (-0.234 to 0.966)

max_real[94] (-0.966 to -0.722)

max_imag[95] (-0.722 to 0.181)

max_real[95] (-0.234 to 0.966)

max_imag[96] (-0.966 to -0.722)

max_real[96] (-0.722 to 0.181)

max_imag[97] (-0.722 to 0.181)

max_real[97] (-0.234 to 0.966)

max_imag[98] (-0.234 to 0.966)

max_real[98] (-0.966 to -0.722)

max_imag[99] (-0.722 to 0.181)

max_real[99] (-0.234 to 0.966)

max_imag[100] (-0.966 to -0.722)

max_real[100] (-0.722 to 0.181)

What about the input network ?

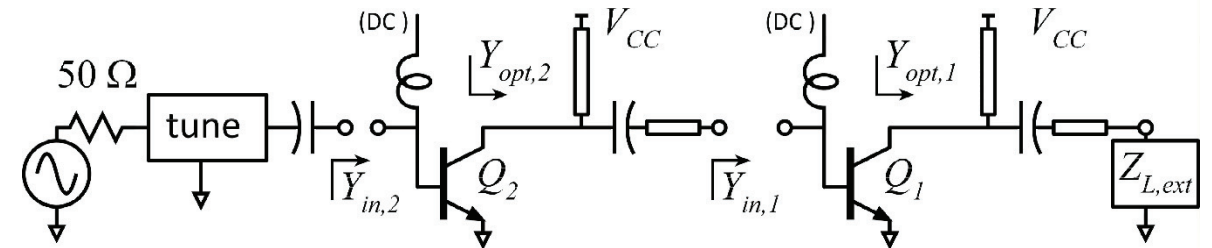
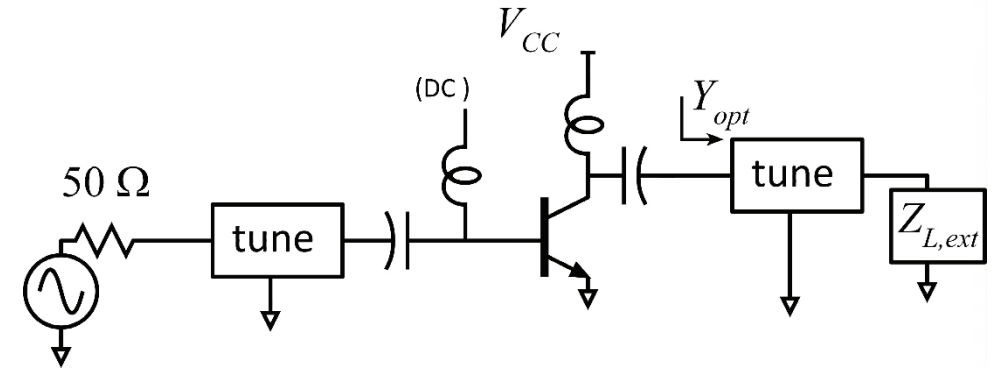
Thus far, we have considered only the output tuning network.

What about the input tuning network ?

To answer this, consider a multi-stage power amplifier.

Each cascaded stage, to be most efficient, must be loaded in its own optimum impedance

The input matching network design of Q_1 is now clear.



Considering a multi-stage power amplifier however immediately raises other concerns...

Multi-stage power amplifiers: power distribution

Assume for Q_1 :

@ $P_{out1} = 0$ dBm (small signal), $P_{in1} = -12$ dBm (12 dB gain) and PAE is low.

@ $P_{out1} = 17$ dBm, $P_{in1} = 6$ dBm (11 dB gain; 1 dB compression) and PAE=20%

@ $P_{out1} = 20$ dBm, $P_{in1} = 10$ dBm (10 dB gain; 2 dB compression) and PAE=PAE_{MAX}=30%

Design for maximum overall PAE:

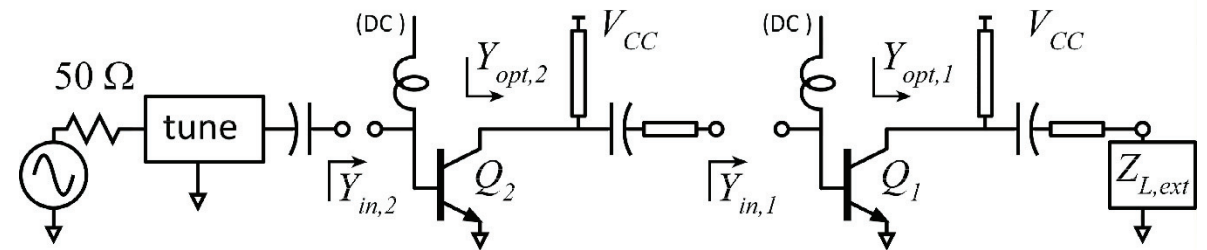
both stages must simultaneously operate at peak PAE.

→ Q_2 must reach peak PAE with $P_{out2} = 10$ dBm.

→ $A_{E2} = A_E / 10$

→ @ $P_{out2} = 10$ dBm, $P_{in2} = 0$ dBm (10 dB gain) and PAE=PAE_{MAX}=30%

→ @ $P_{out2} = 0$ dBm (small signal), $P_{in2} = -12$ dBm (12 dB gain) and PAE is low.



2-stage amplifier:

@ $P_{out1} = 20$ dBm, $P_{in2} = 0$ dBm (20 dB total gain); **30% PAE for each stage; 30% overall PAE**

@ $P_{out1} = 0$ dBm (small signal), $P_{in2} = -24$ dBm (24 dB gain).

4 dB gain compression between small-signal and peak PAE

Multi-stage power amplifiers: driver stage sizing

Assume for Q_1 :

@ $P_{out1} = 0$ dBm (small signal), $P_{in1} = -12$ dBm (12 dB gain) and PAE is low.

@ $P_{out1} = 17$ dBm, $P_{in1} = 6$ dBm (11 dB gain; 1 dB compression) and PAE=20%

@ $P_{out1} = 20$ dBm, $P_{in1} = 10$ dBm (10 dB gain; 2 dB compression) and PAE=PAE_{MAX}=30%

Design for less gain compression:

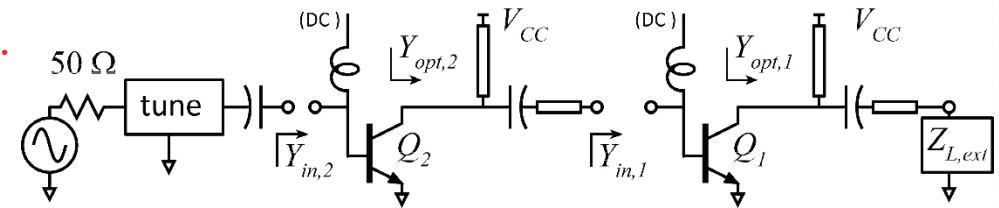
size Q_2 such that Q_2 has 1 dB compression when Q_1 has 2 dB compression.

→ Q_2 must reach 1 dB gain compression with $P_{out2} = 10$ dBm.

→ $A_{E2} = A_E / 5$

→ @ $P_{out2} = 10$ dBm, $P_{in2} = -1$ dBm (11 dB gain) and PAE=20%

→ @ $P_{out2} = 0$ dBm (small signal), $P_{in2} = -12$ dBm (12 dB gain) and PAE is low.



2-stage amplifier:

@ $P_{out1} = 20$ dBm, $P_{in2} = -1$ dBm (21 dB total gain); PAE₁ = 30%; PAE₂ = 20% → PAE_{overall} = $(P_{out1} - P_{in2}) / (P_{DC1} + P_{DC2}) = 28.7\%$

@ $P_{out1} = 0$ dBm (small signal), $P_{in2} = -24$ dBm (24 dB gain).

3 dB gain compression between small-signal and peak PAE

Over-sized driver stages

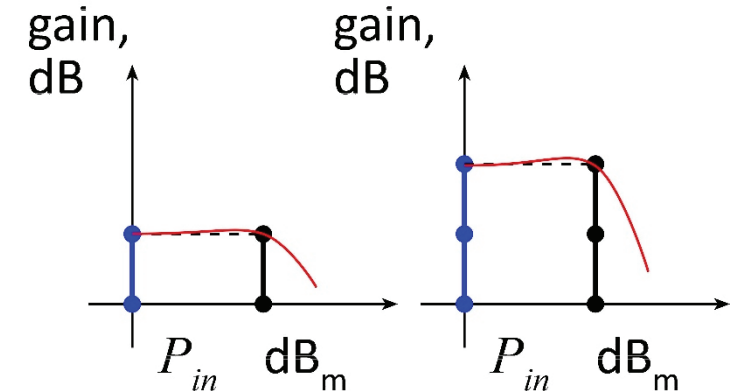
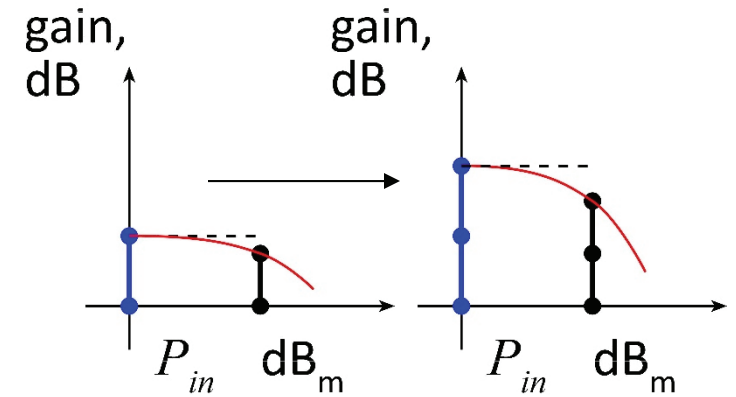
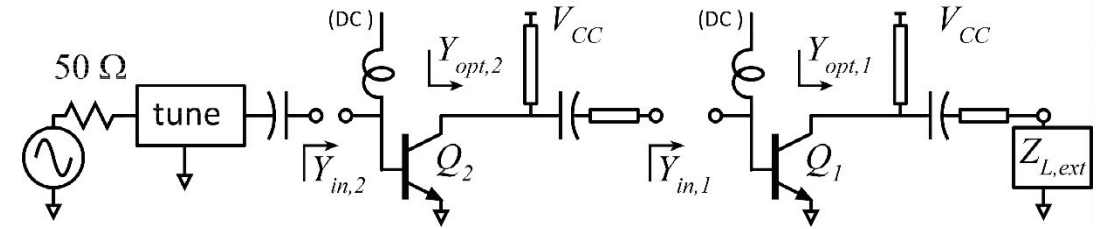
In a multi-stage amplifier, if driver stages are sized for peak PAE, then gain compression at PAE will increase rapidly as the number of stages is increased to increase the overall gain.

Over-sizing the driver stages will reduce the accumulated gain compression, but will reduce the overall PAE.

Adaptive bias circuits can be used in some systems to flatten the $\text{dB}(P_{out})$ vs. $\text{dB}(P_{in})$ characteristics.

Overall digital pre-distortion can also be applied.

These are advanced topics, but important ones.



Multi-stage PAs: I_{\max} , Z_{load} , transistor size problems

Consider this 2-stage amplifier:

$$P_{\text{out}1} = 1000 \text{ mW}; P_{\text{in}1} = 100 \text{ mW};$$

$$P_{\text{out}2} = 100 \text{ mW}; P_{\text{in}2} = 10 \text{ mW}$$

Assume $(V_{\max} - V_{\min}) = 4$ Volts and recollect that

$$Z_L = 1/Y_L = R_L + j0\Omega = (V_{\max} - V_{\min}) / I_{\max}$$

$$I_{\text{DC}} = I_{\max} / 2$$

$$P_{\text{RF,max}} = (V_{\max} - V_{\min}) I_{\max} / 8 = (V_{\max} - V_{\min})^2 / 8R_L$$

BJTs or FETs with $J_{\max} = 2 \text{ mA}/\mu\text{m}$ current density

Then

Stage 1: $I_{\text{DC}} = 1 \text{ A}$; $R_L = 2 \Omega$; $N_G W_G$ or $N_E L_E = 1000 \mu\text{m}$

Stage 2: $I_{\text{DC}} = 100 \text{ mA}$; $R_L = 20 \Omega$; $N_G W_G$ or $N_E L_E = 100 \mu\text{m}$

Extremely low load impedances, extremely high currents, extremely large transistor sizes.

This is the microwave power-combining problem

