ECE 145C / 218C, notes set xx: frequency multipliers.

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Frequency multiplier:

Local oscillator generated by:

PLL

Frequency multiplier chain

....or a combination of these.

Why PLLs?

avoids spurious harmonics

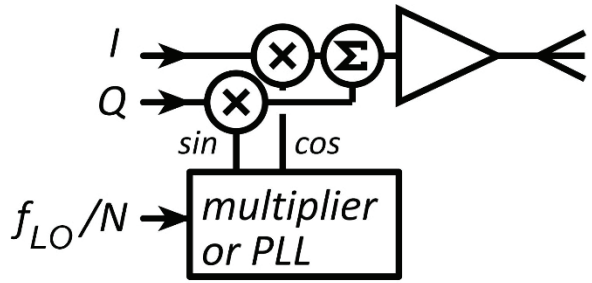
frequency synthesis

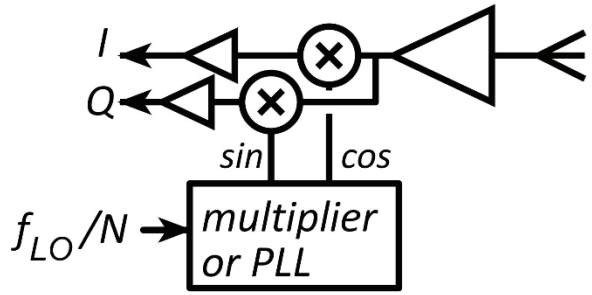
frequency synchronization

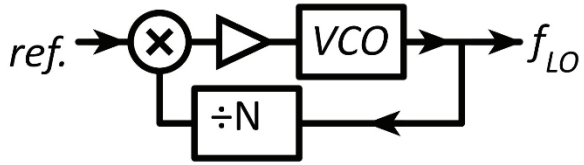
phase synchronization

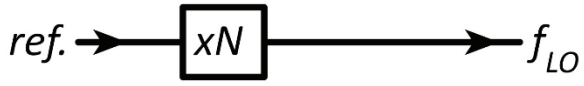
Why multipliers ?

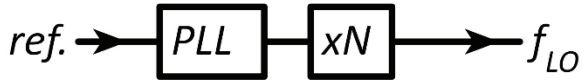
can* be lower phase noise...











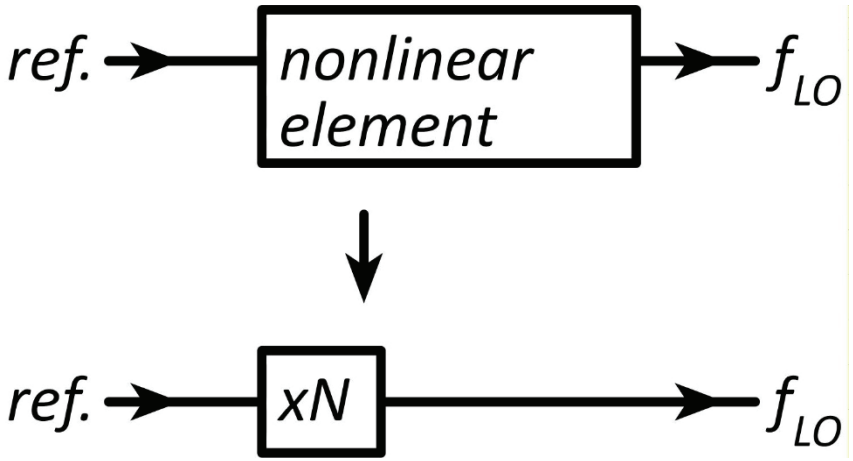
*considerations are involved. Depends upon achievable VCO and PLL phase noise at f_{LO} vs. at f_{LO}/N.

Frequency multiplier = nonlinear element

$$V_{in}(t) = V_{in,0}\cos(\omega_{in}t)$$

$$V_{out}(t) = a_0 + a_1 V_{in} + a_2 V_{in}^2 + a_3 V_{in}^3 + \ldots$$

(recollect units of $a_0, a_1, a_2, \ldots$)



$a_0 \rightarrow$ fixed amplitude, frequency = DC = $0\omega_{in}$

$a_1 V_{in} \rightarrow$ amplitude $\propto a_1 V_{in}^1$, frequency = $1\omega_{in}$

$a_2 V_{in}^2 \rightarrow$ amplitude $\propto a_2 V_{in}^2$, frequencies = $0\omega_{in}, 2\omega_{in}$

$a_3 V_{in}^3 \rightarrow$ amplitude $\propto a_3 V_{in}^3$, frequencies = $1\omega_{in}, 3\omega_{in}$

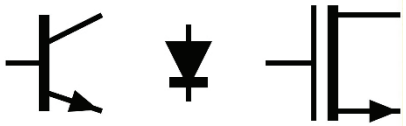
$a_4 V_{in}^4 \rightarrow$ amplitude $\propto a_4 V_{in}^4$, frequencies = $0\omega_{in}, 2\omega_{in}, 4\omega_{in}$

$a_5 V_{in}^5 \rightarrow$ amplitude $\propto a_5 V_{in}^5$, frequencies = $1\omega_{in}, 3\omega_{in}, 5\omega_{in}$

etc.

Any nonlinear element will generate harmonics

Driven hard, any nonlinear will generate many harmonics



Spurious Harmonics = "Spurs"

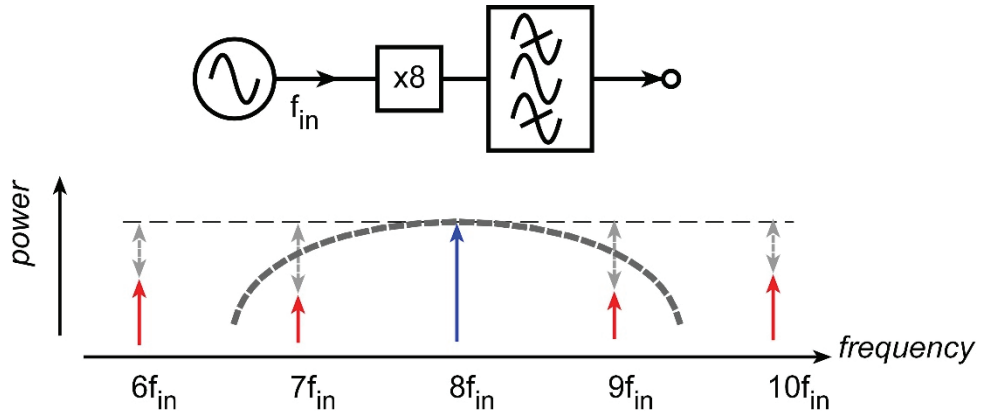
Multiplier will generate many harmonics

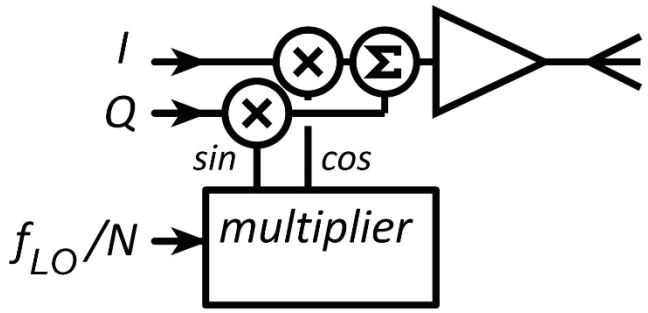
wanted = :-)

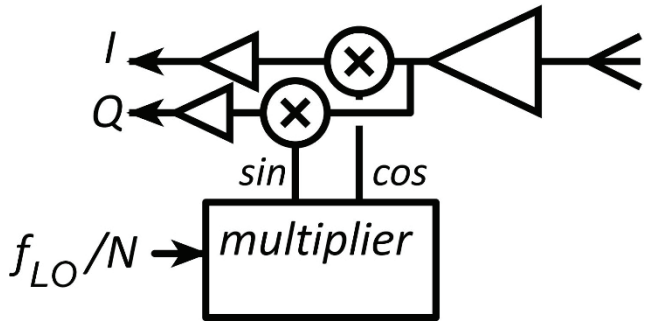
unwanted = spurious = "spurs"

In this example, the transmitter,
designed to transmit at $f_{RF} = 8 f_{in}$
will also radiate at $7 f_{in}$ and $9 f_{in}$.
→ Potential interference with other services.
→ Potential FCC license violation.

In this example, the receiver,
designed to receive at $f_{RF} = 8 f_{in}$
will also receive at $7 f_{in}$ and $9 f_{in}$.
→ Potential receiver interference
from signals in
nearby frequency bands.



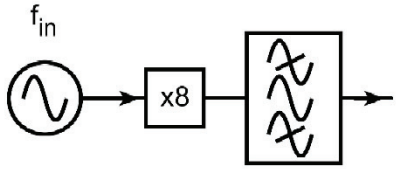


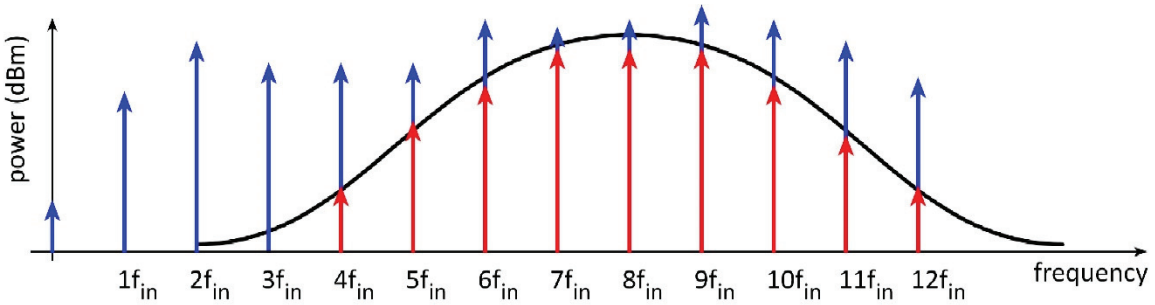


Low-order multipliers: easier to suppress "spurs"

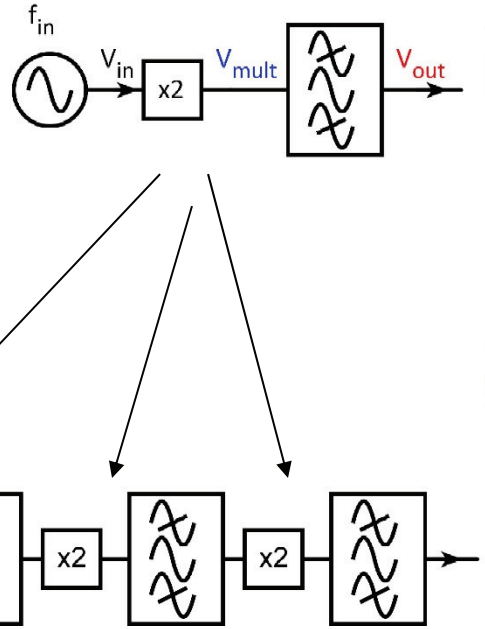
Given filters of some maximum feasible $Q = \Delta f_{3dB} / f_o, \ldots$

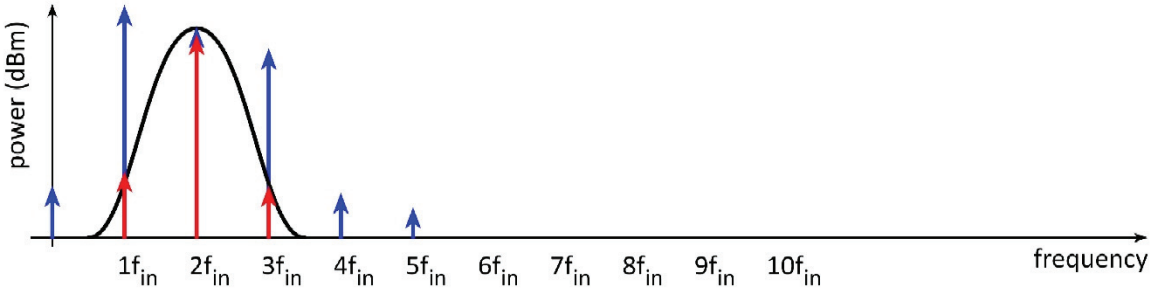
It is more difficult to suppress spurious harmonics a single high-order multiplier...

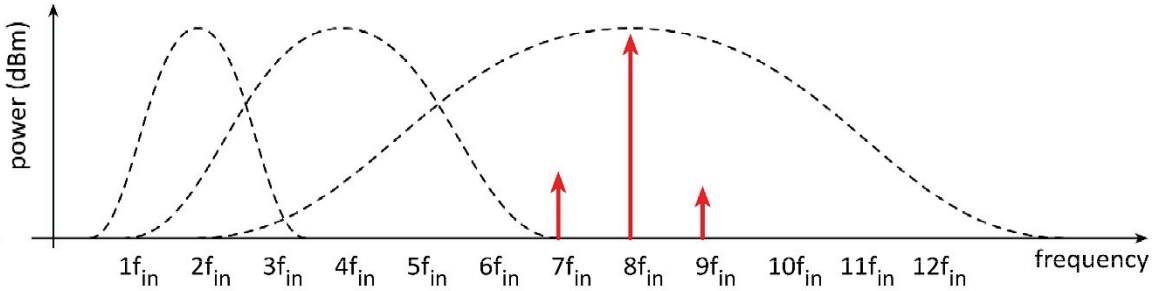




...than in a in a chain of low-order multipliers.







3rd-harmonic generation by overdriven amplifier (1)

An overdriven amplifier is nonlinear.

If symmetric:

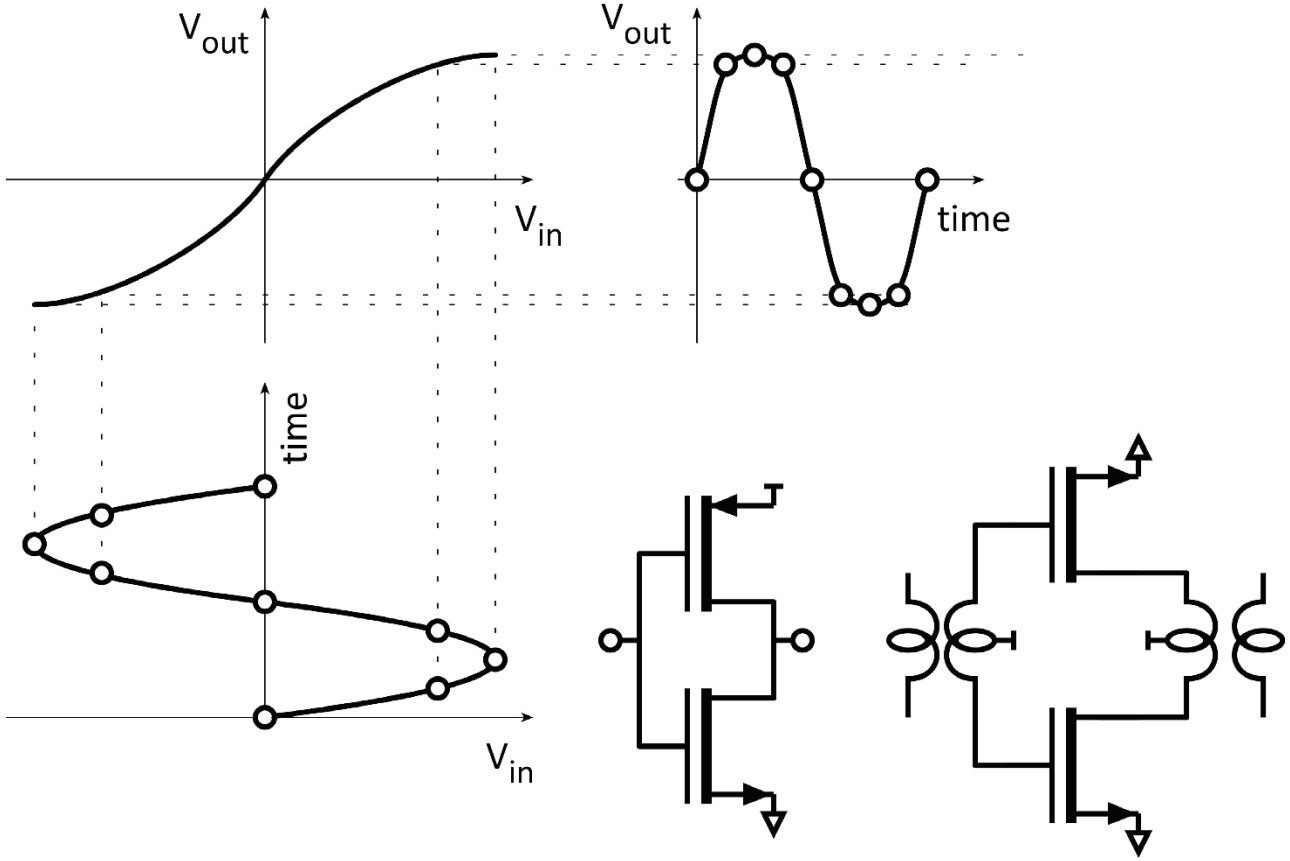
suppressed $a_2 V_{in}^2, a_4 V_{in}^4, \ldots$terms

suppressed $2\omega_{in}, 4\omega_{in}, \ldots$. generation

even harmonic are suppressed.

Imperfect symmetry:

$\rightarrow$ nonzero even-harmonic generation.



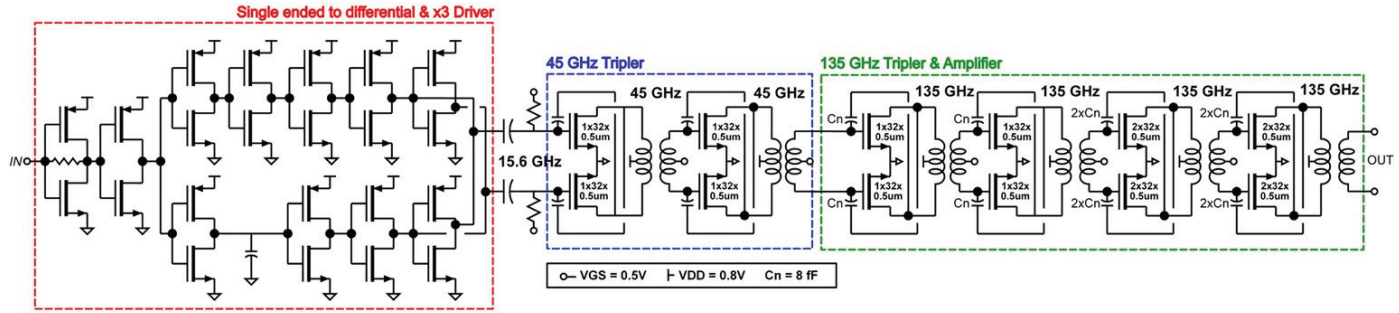
3rd-harmonic generation by overdriven amplifier (2)

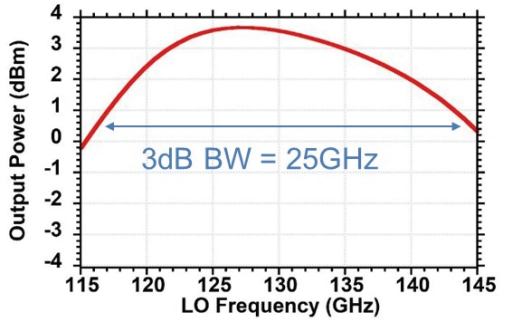
Implementation: 22 nm SOI CMOS (Globalfoundries 22FDX)

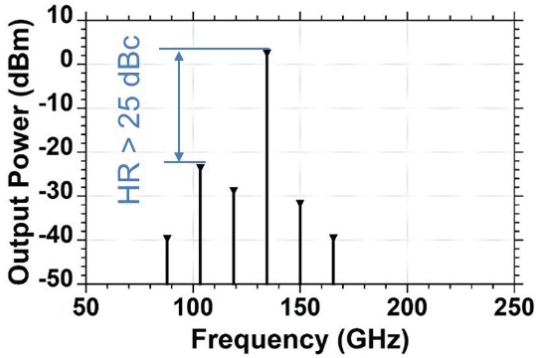
Input buffer:
cascaded CMOS inverters.

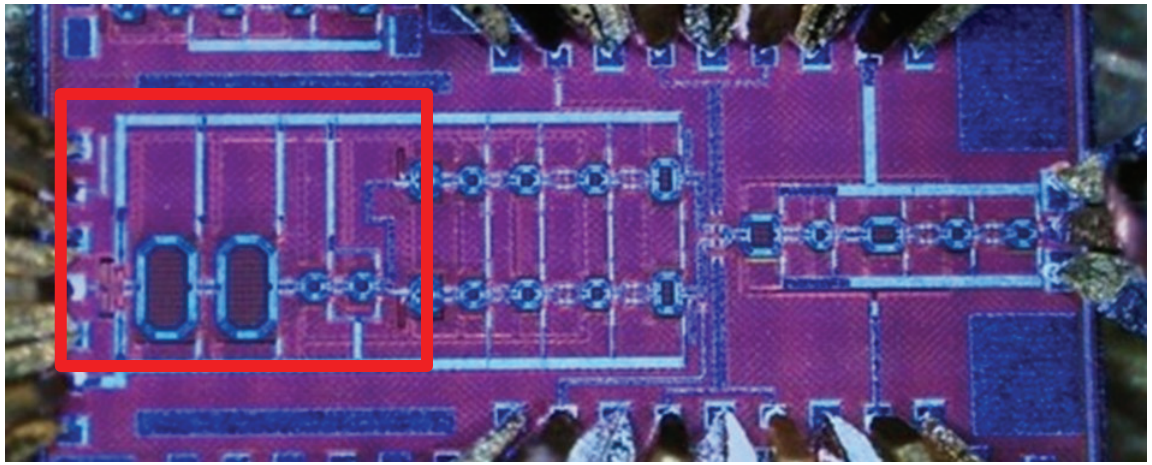
1st frequency tripler: 15GHz to 45 GHz pseudodifferential CMOS tuned amplifier

2nd frequency tripler: 45GHz to 155 GHz pseudodifferential CMOS tuned amplifier









Farid et. al, 2019 IEEE International Microwave Symposium

Push-push frequency doubler (1)

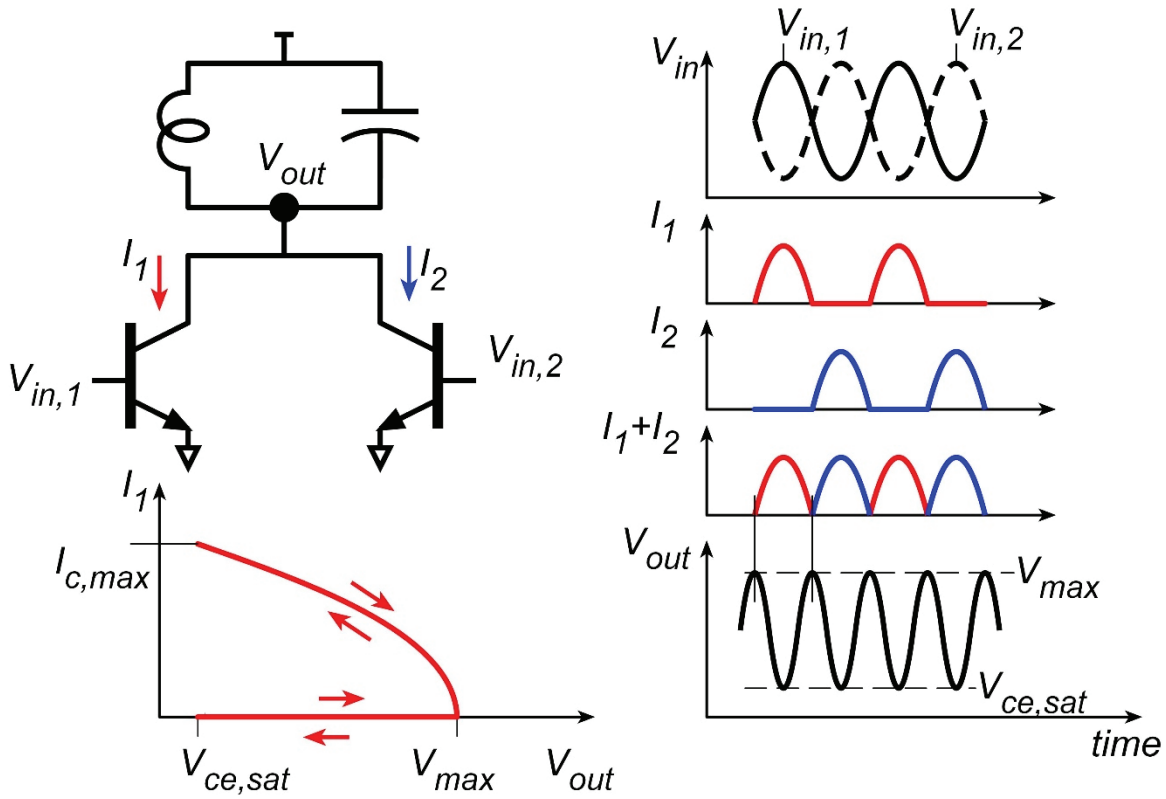
Differential (out-of-phase) inputs

Each transistor biased at cutoff

Each transistor: half-wave rectifier
Strong even-harmonic generation

(nearly) symmetric circuit
(nearly) suppresses odd harmonics

The illustrated *large-signal* loadline provides the greatest *saturated* 2nd-harmonic output power.



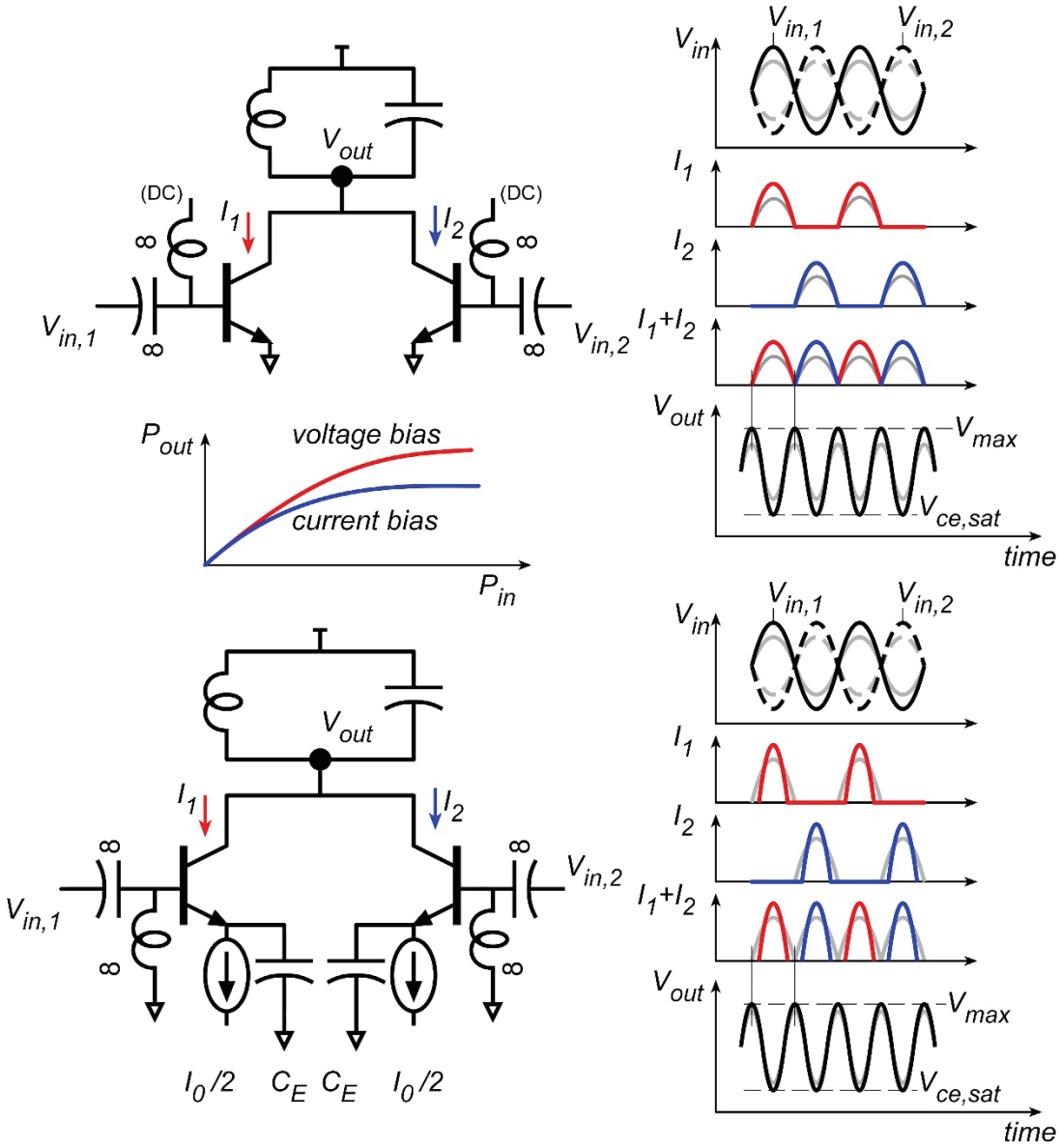
Push-push frequency doubler (2)

More details

The bottom circuit forces
a time-average output current
independent of P_{in}.

$\rightarrow$ Better regulation of P_{out}

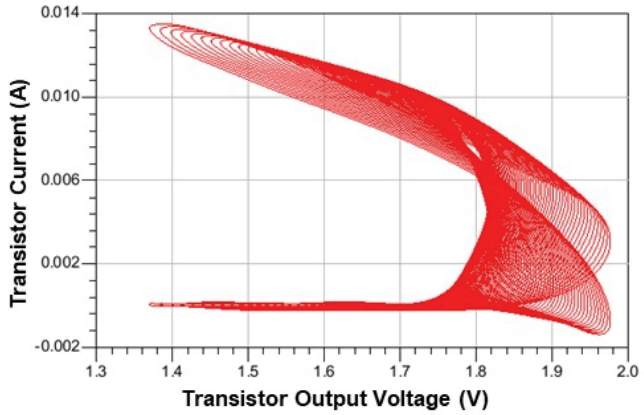
Key design challenge:
maintaining symmetry
(hence odd-harmonic supression)
even with
...unequal (V_{in}^{+}, V_{in}^{-}) input signals
...imperfectly matched transistors.

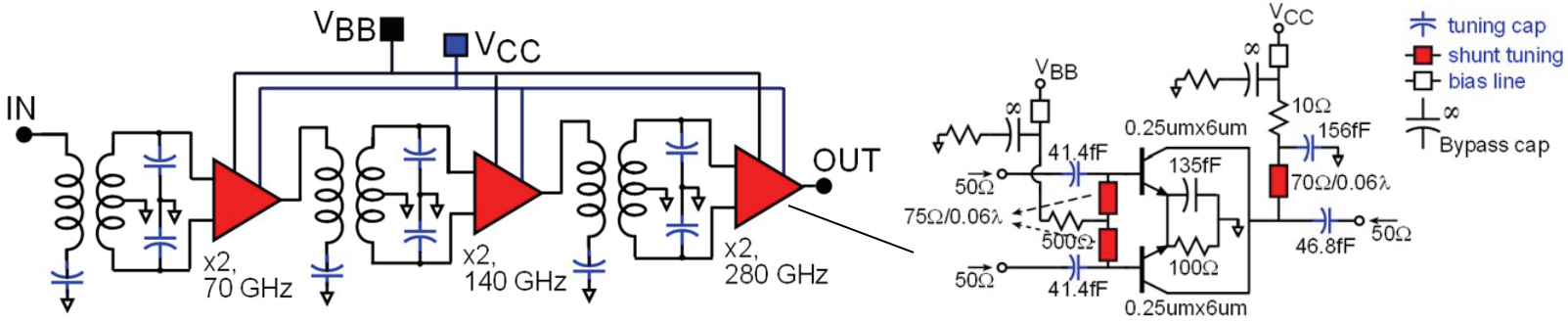


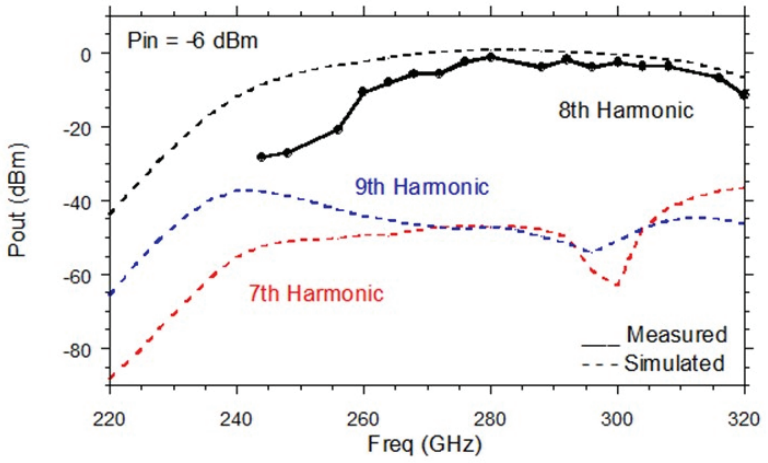
Push-push frequency doubler (3)

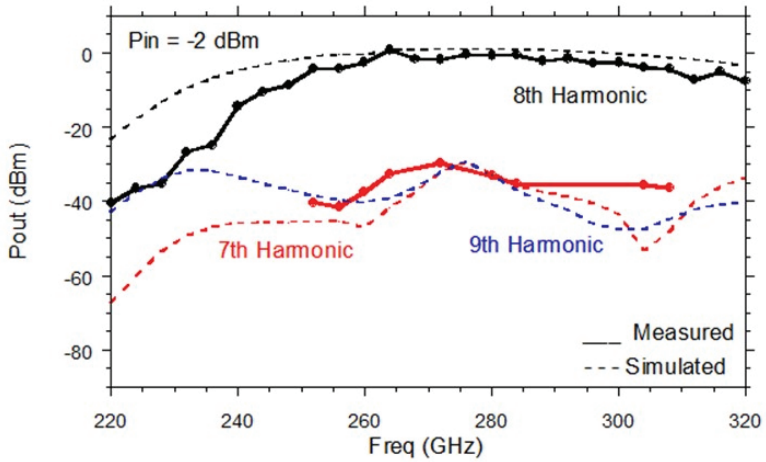
8 : 1 multiplier (35 GHz to 280 GHz)

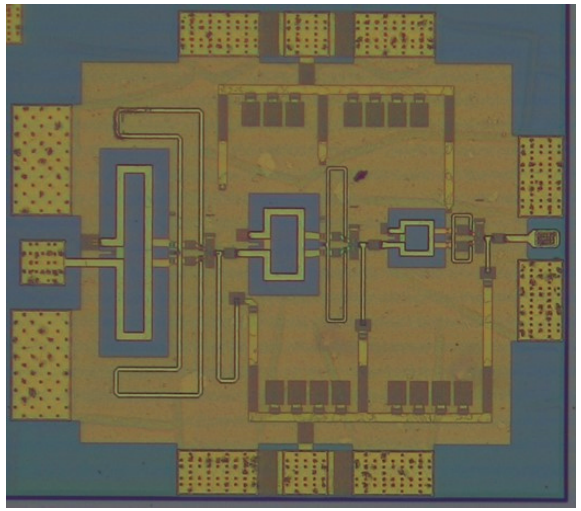
Soylu et. al, IEEE Journal of Solid-State Circuits, 2023





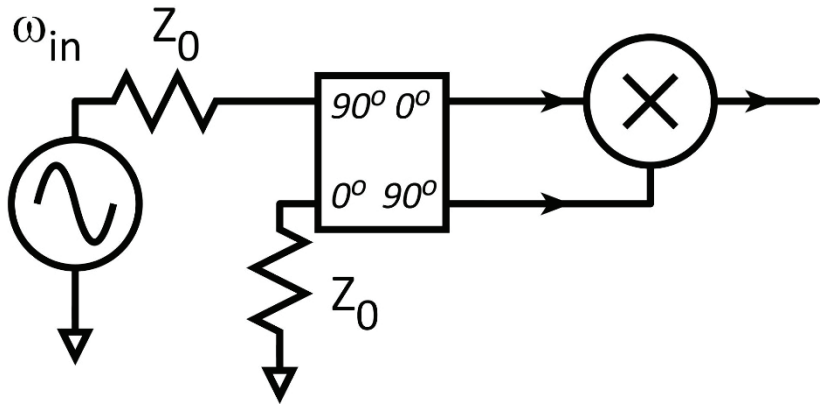






Mixer as Frequency Doubler

Needs: mixer and 90 degree phase splitter



Mixer inputs:

$$2V_{RF}(t) = 2V_{RF}\cos(\omega_{in}t) = V_{RF}(z_{in} + 1/z_{in})$$

$$2jV_{LO}(t) = 2jV_{LO}\sin(\omega_{in}t) = V_{LO}(z_{in} - 1/z_{in})$$

Mixer output (γ has units of 1/Volts)

$$V_{out}(t) = \gamma V_{RF}(t)V_{LO}(t)$$

$$4jV_{out}(t) = 4j\gamma V_{RF}(t)V_{LO}(t) = V_{RF}V_{LO}\gamma(z_{in} + 1/z_{in})(z_{in} - 1/z_{in})$$

$$4jV_{out}(t) = V_{RF}V_{LO}\gamma(z_{in}^2 + 1 - 1 - 1/z_{in}^2) = V_{RF}V_{LO}\gamma(z_{in}^2 - 1/z_{in}^2) = 2jV_{RF}V_{LO}\gamma\sin(2\omega_{in}t)$$

$$V_{out}(t) = \frac{V_{RF}V_{LO}\gamma}{2}\sin(2\omega_{in}t)$$

Caution: if phase shift is *not exactly* 90^0, then circuit will generate odd harmonics

XOR gate as Frequency Doubler

This is very similar to the analog mixer design.

Digital (limited) vs. analog (continuous) multiplication

Spurious harmonics will arise from

1) imperfect 90^0 phase shift.

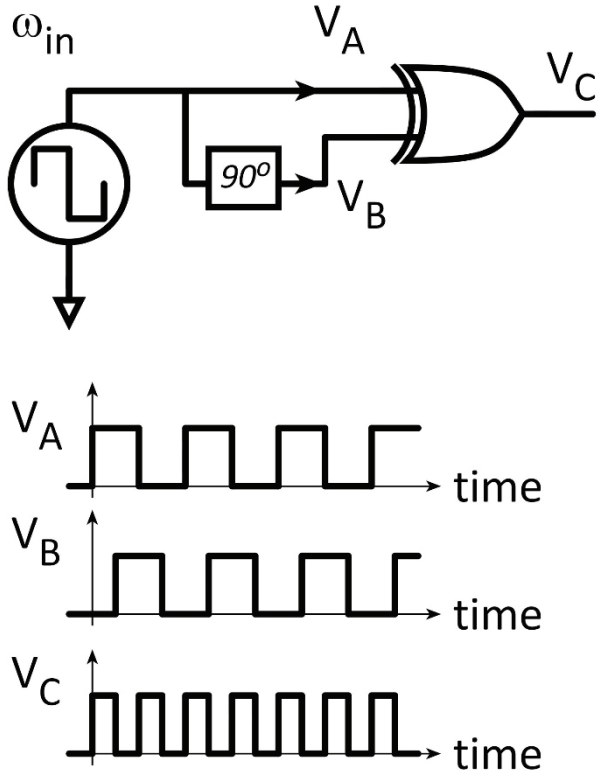
2) input not exactly 50% of the time high, 50% of the time low.

There are methods* to suppress these errors using

DC negative feedback loops.

XOR multiplier designs will likely be power-efficient only for

relatively low-frequency designs....for which there are other options.



*S. Kim, A. Simsek, M. Urteaga and M. J. W. Rodwell, "High-Spurious-Harmonic-Rejection 32-53 GHz and 50-106 GHz Frequency Doublers using Digital Logic and DC Negative Feedback, European Radar Conference (EuRAD), Madrid, 26-28 Sept. 2018