ECE 145C / 218C, notes set xx: Power Combining

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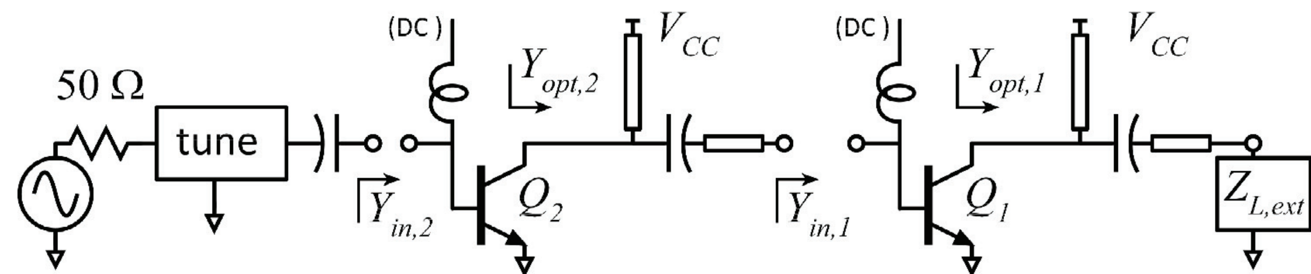
Multi-stage PAs: I_{max}, Z_{load}, transistor size problems

Consider this 2-stage amplifier:

$P_{out1} = 1000$ mW; $P_{in1} = 100$ mW;

$P_{out2} = 100$ mW; $P_{in2} = 10$ mW



Assume $(V_{max} - V_{min}) = 4$ Volts and recollect that

$Z_L = 1/Y_L = R_L + j0\Omega = (V_{max} - V_{min})/I_{max}$

$I_{DC} = I_{max}/2$

$P_{RF,max} = (V_{max} - V_{min})I_{max}/8 = (V_{max} - V_{min})^2/8R_L$

Assume BJTs or FETs with $J_{max} =$ 2 mA/μm current density

Then

Stage 1: $I_{DC} = 1$ A; $R_L = 2\ \Omega$; $N_G W_G$ or $N_E L_E = 1000\ \mu$m

Stage 2: $I_{DC} = 100$ mA; $R_L = 20\ \Omega$; $N_G W_G$ or $N_E L_E = 100\ \mu$m

Extremely low load impedances, extremely high currents,extremely large transistor sizes.

This is the microwave power-combining problem

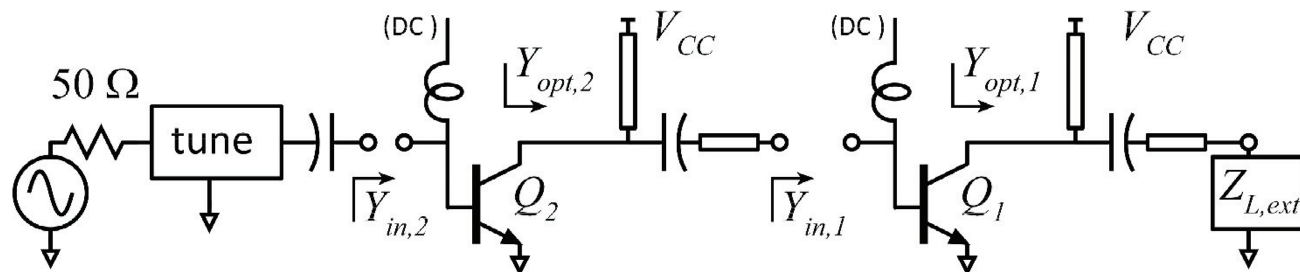
Low impedances, high currents, big transistors

The impedance problem:

$P_{RF,\max} = (V_{\max} - V_{\min}) I_{\max} / 8 = (V_{\max} - V_{\min})^2 / 8 R_L$

$Z_L = (V_{\max} - V_{\min}) / I_{\max}$

$\rightarrow Z_L = (V_{\max} - V_{\min})^2 / 8 P_{RF,\max}$ Very low load impedance.



The current problem:

$P_{RF,\max} = (V_{\max} - V_{\min}) I_{\max} / 8 = (V_{\max} - V_{\min})^2 / 8 R_L$

$\rightarrow I_{\max} = 8 P_{RF,\max} / (V_{\max} - V_{\min})$ Very high current; many transistor fingers

Transistor maximum finger length (1)

FET:

Gate resistance per finger $R_{G,finger} = k_1 W_g$

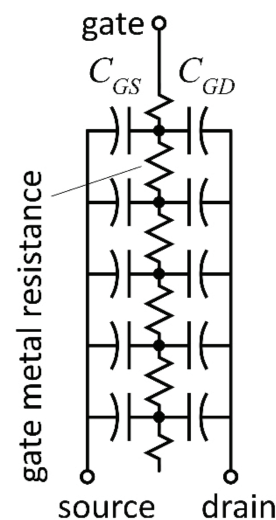
Gate resistance, N_g parallel fingers $R_G = k_1 W_g / N_g$

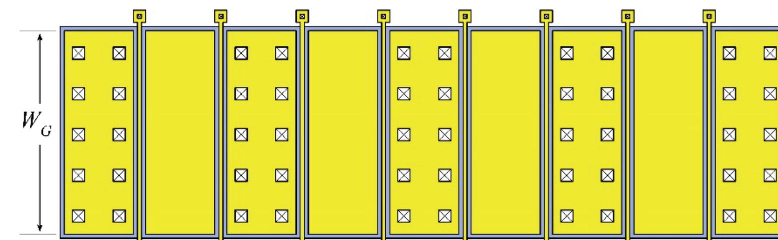
To avoid degrading $f_{\max}$, need $R_G < (R_g + R_s)$

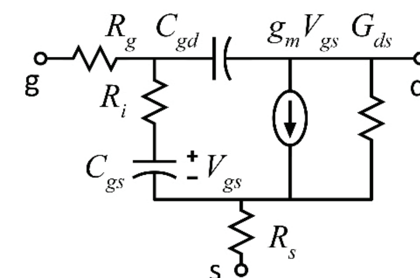
But $(R_g + R_s) = k_2 / N_g W_g$,

$k_1 W_g / N_g < k_2 / N_g W_g$

Maximum finger length $W_{g,\max} < \sqrt{k_2 / k_1}$







Bipolar:

Base metal resistance per finger $R_{BB,metalfinger} = k_1 L_E$

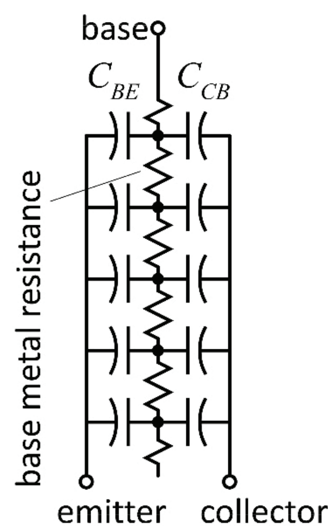
Base metal resistance, N_E parallel fingers $R_{BB,metal} = k_1 L_E / N_E$

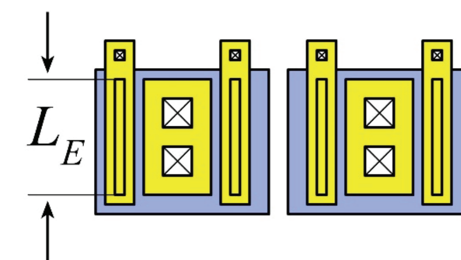
To avoid degrading $f_{\max}$, need $R_{bb,metal} < (R_{bb} + R_{ex})$

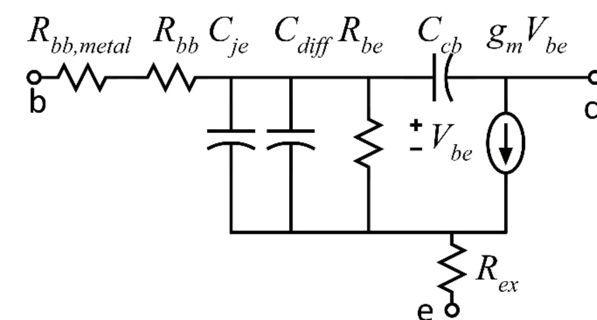
But $(R_{bb} + R_{ex}) = k_2 / N_E L_E$,

$k_1 L_E / N_E < k_2 / N_E L_E$

Maximum finger length $L_{E,\max} < \sqrt{k_2 / k_1}$





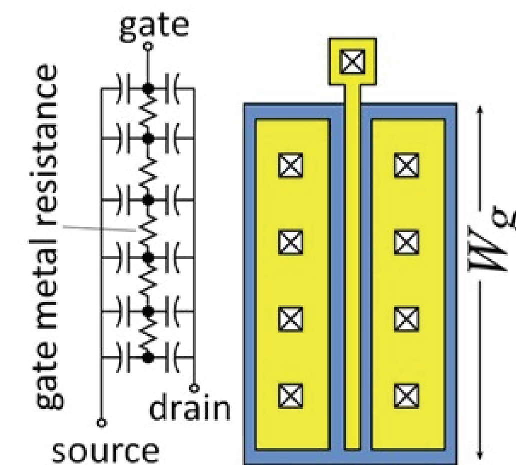


Transistor maximum finger length (2)

If we can allow $f_{\max}$ to be degraded by the metal finger resistance

with $f_{\max}\big|_{\text{with_metal_finger_resistance}} = k_3 f_{signal}$ $(k_3 > 1!)$

then we can design the transistor multi-finger layout differently



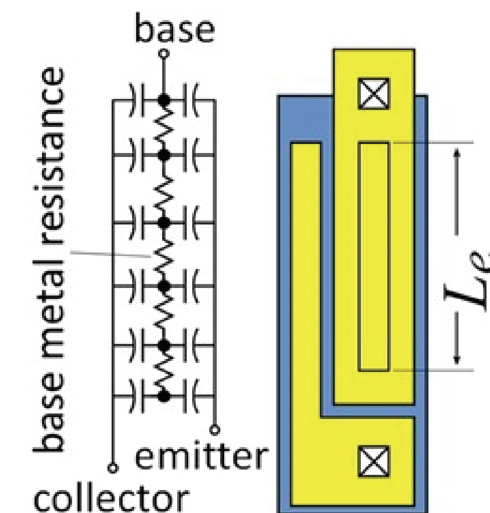
FET: gate metal resistance charging time $= R_{metal}(C_{gs} + C_{gd}) \propto$ (finger length)^2

BJT: base metal resistance charging time $= R_{metal}(C_{be} + C_{cb}) \propto$ (finger length)^2

Since $R_{metal}(C_{gs} + C_{gd})$ (FET) or $R_{metal}(C_{be} + C_{cb})$ (Bipolar) will be one term in $f_{\max}$,

$f_{\max}\big|_{\text{with_metal_finger_resistance}} = k_3 f_{signal}$ implies that $R_{metal}(C_{gs} + C_{gd}) \propto 1/f_{signal}$

$f_{\max}\big|_{\text{with_metal_finger_resistance}} = k_3 f_{signal}$ implies that $R_{metal}(C_{be} + C_{cb}) \propto 1/f_{signal}$



Given this assumption

Maximum finger length $\propto 1/\sqrt{f_{signal}}$

Current per finger $\propto 1/\sqrt{f_{signal}}$

High Power: Many transistor fingers

$P_{RF,\max} = (V_{\max} - V_{\min})I_{\max} / 8 \rightarrow I_{\max} = 8P_{RF,\max} / (V_{\max} - V_{\min})$

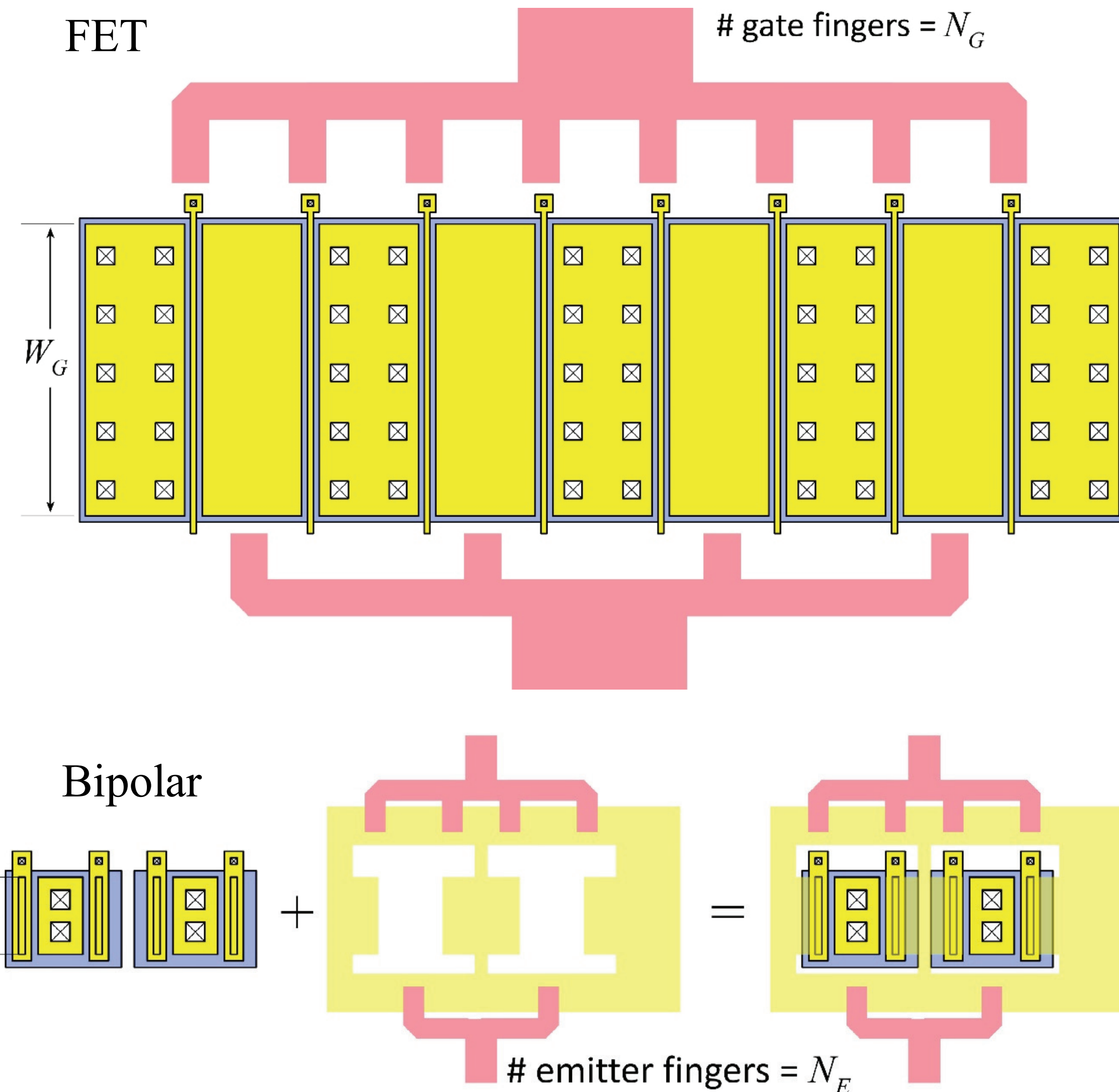
But $I_{\max} = N_E L_E J_{E,\max}$ (Bipolars) or $N_G W_G J_{S,\max}$ (FET)

$N_E L_E = 8P_{RF,\max} / J_{E,\max}(V_{\max} - V_{\min})$ Bipolars

$N_G W_G = 8P_{RF,\max} / J_{s,\max}(V_{\max} - V_{\min})$ FETs

Given that there is also a maximum finger length $(L_{E,\max}, W_{g,\max})$, high-power transistors must have many fingers.

The multi-finger feed network then degrades the transistor $(f_\tau, f_{\max})$.



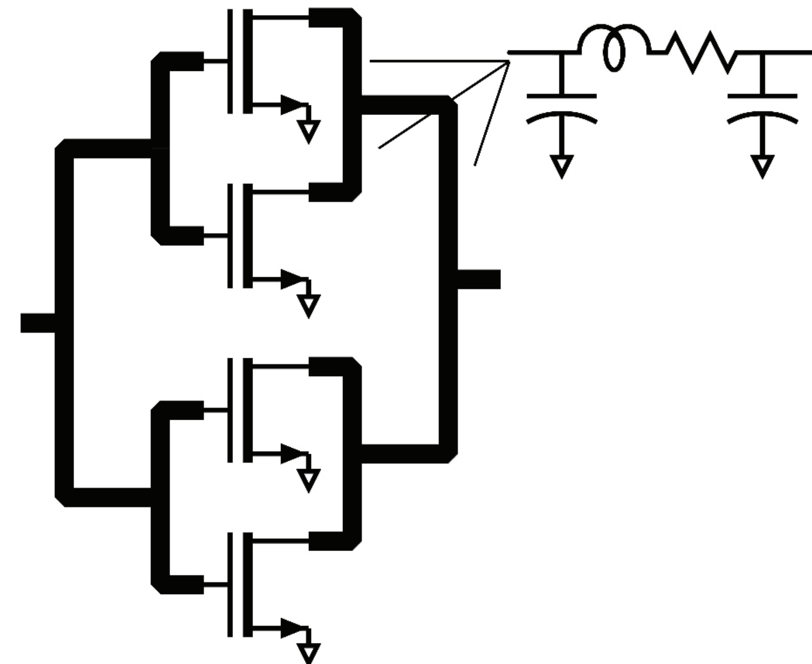
Multi-finger transistor feed network parasitics

The finger-finger interconnects can be modelled as either transmission-lines or lumped *RLC* networks.

Transistor $(f_\tau, f_{\max})$ will be degraded

Can we avoid this ?

The answer: only in part.



Multi-finger transistor feed network parasitics

Can we avoid degrading $(f_\tau, f_{\max})$ by using impedance-matched lines ?

Transistor with N_G (or N_E) fingers. Load impedance at end of each line: $Z_{end} = N_G Z_{Load}$

Transistor cell with internal matched-impedance interconnects: $Z_{L,finger} = Z_{end}$ which requires $Z_{line} = Z_{L,finger} = Z_{end} = N_G Z_{Load}$

But note:

1) realizable on-chip transmission-lines have $Z_{line,\max} \approx 80-90\ \Omega$

2) $Z_{L,finger} = \begin{cases} (V_{\max} - V_{\min}) / J_{S,\max} W_E & \text{FETs} \\ (V_{\max} - V_{\min}) / J_{E,\max} L_E & \text{Bipolars} \end{cases}$

3) 240 nm InP HBT: $(V_{\max} - V_{\min}) \cong 3.5\text{V}$;

$J_{E,\max} \cong 3\ \text{mA}/\mu\text{m},\ L_{E,\max} \approx 6\ \mu\text{m} \ @ f_{signal} = 250\ \text{GHz}$

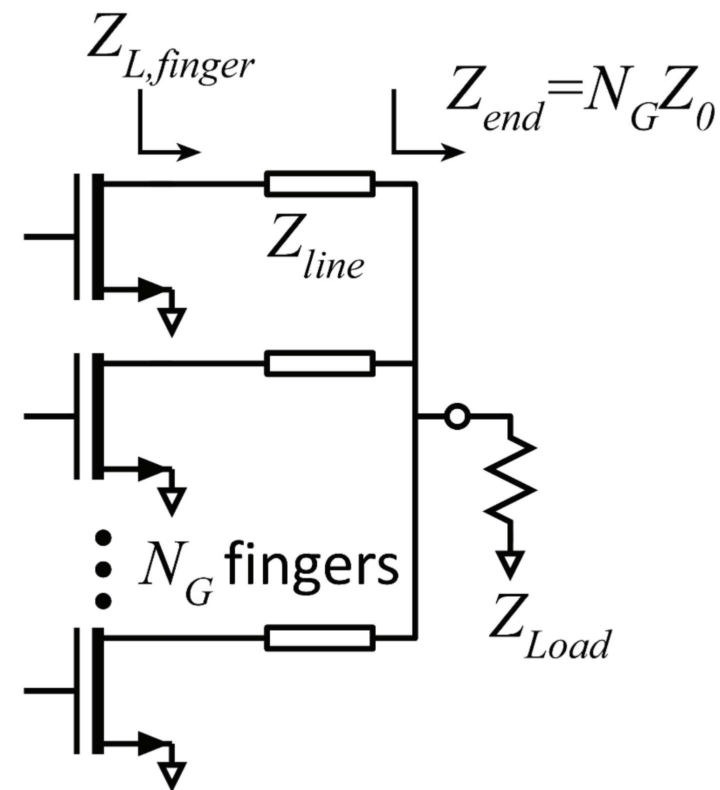
$\rightarrow Z_{L,finger} = 194\ \Omega$

3) W-band GaN HEMT : $(V_{\max} - V_{\min}) \cong 25\text{V}$;

$J_{E,\max} \cong 1.67\ \text{mA}/\mu\text{m},\ W_{G,\max} \approx 30\ \mu\text{m} \ @ f_{signal} = 94\ \text{GHz}$

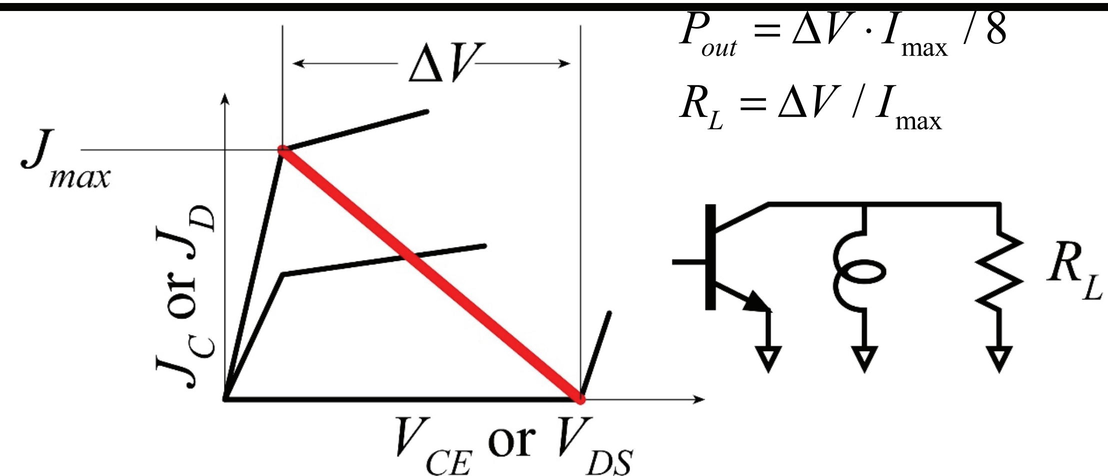
$\rightarrow Z_{L,finger} = 500\ \Omega$

Individual transistor fingers cannot be connected with impedance-matched interconnects



Transistor layouts: *I*, *V*, *Z*, and *P*.

R_L below 25 Ω or above 75 Ω is hard to realize.

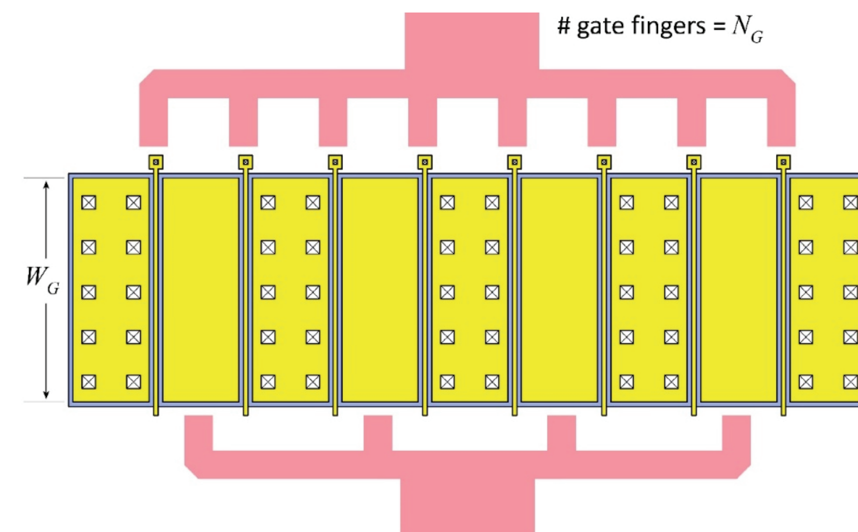


$$I_{max} = \frac{\Delta V}{R_L} = J_{max} \cdot \text{(number fingers)(finger length)};$$

$$\rightarrow \text{(number fingers)(finger length)} = \frac{\Delta V}{J_{max} R_L}$$

Large ΔV, small J_{max}, or small R_L:

long fingers or many fingers $\rightarrow$ layout parasitics $\rightarrow$ lower f_{max}.



Higher frequencies need smaller layout parasitics

$\rightarrow$ shorter fingers ($\text{length}_{max} \propto f^{-1/2}$), fewer fingers ($\#_{max} \propto f^{-1}$)

Technologies with high ΔV and low J_{max} are problematic.

Hierarchy: multi-finger transistors & power-combiner

We separate the overall power-combining structure into 3 regions

1) A single transistor finger of the maximum allowable length

$Z_{L,finger} = (V_{\max} - V_{\min}) / J_{E,\max} L_{E,\max}$ (bipolars) or $(V_{\max} - V_{\min}) / J_{S,\max} W_{G,\max}$ (FETs)

for these, $Z_{L,finger} >> Z_{line,\max}$

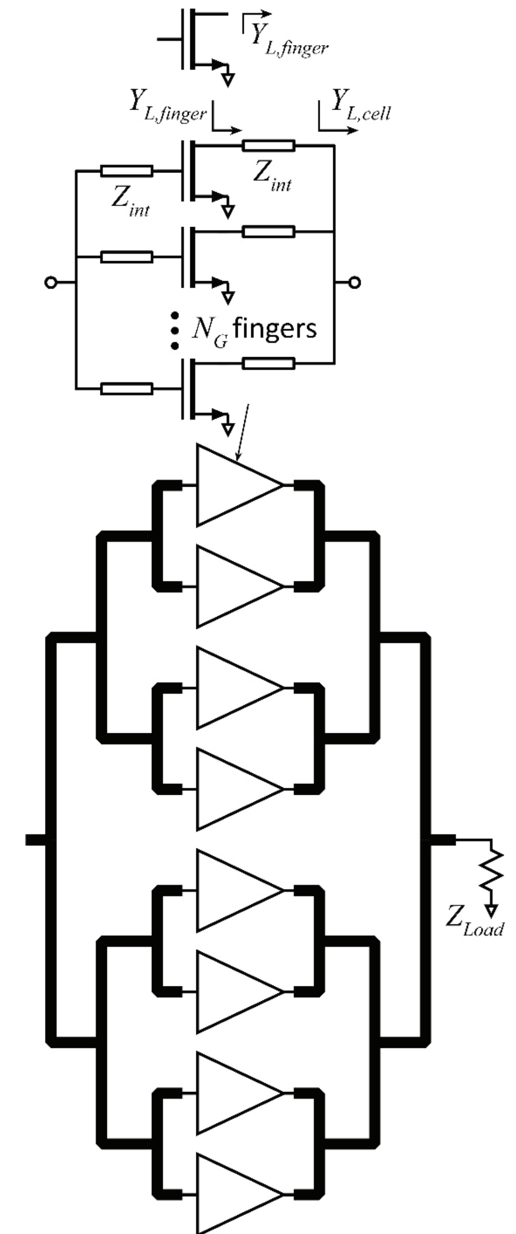
2) multi-finger transistor cells with N_E or N_G fingers.

for these $Y_{L,cell} \approx N_E \dfrac{J_{E,\max} L_{E,\max}}{V_{\max} - V_{\min}} + j\omega C_{out}$ (bipolars) or $N_G \dfrac{J_{s,\max} W_{g,\max}}{V_{\max} - V_{\min}} + j\omega C_{out}$ (FETs)

The cell has $Z_{L,cell} \leq \; Z_{line,\max}$

3) The power-combiner.

With overall load Z_{Load}, each cell is loaded in $Z_{L,cell}$



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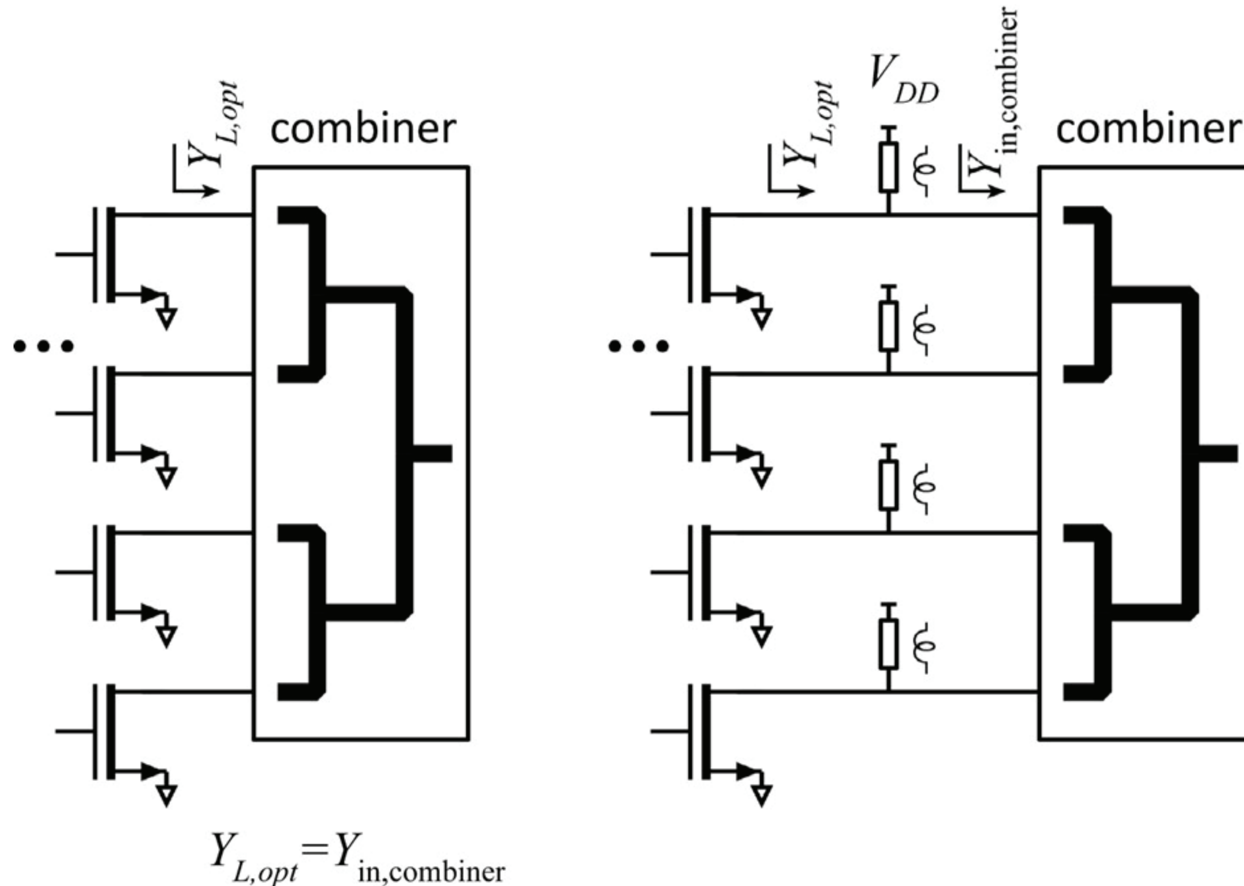
Power Combiners: with and without inductive pre-tuning

$Y_{L,opt} = G_{L,opt} + jB_{L,opt}$;
given transistor capacitances, $jB_{L,opt}$ is usually inductive

Without inductive pre-tuning:
power combiner provides $Y_{L,opt} = G_{L,opt} + jB_{L,opt}$

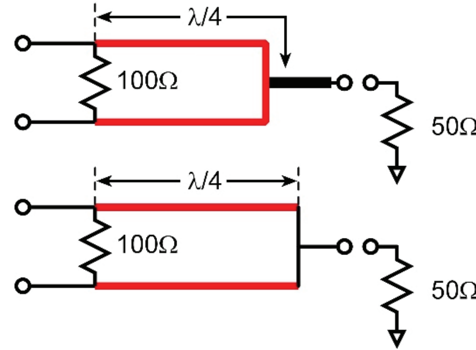
With inductive pre-tuning:
power combiner provides $Y_{in,combiner} = G_{L,opt} + j0$ S



Wilkinson Power-Combiner

Line lengths: $\lambda_g / 4$

Line impedances: $Z_{line} = Z_0 \cdot \sqrt{2}$



$50\Omega \cdot 2^{1/2} = 70.7\Omega$

50Ω

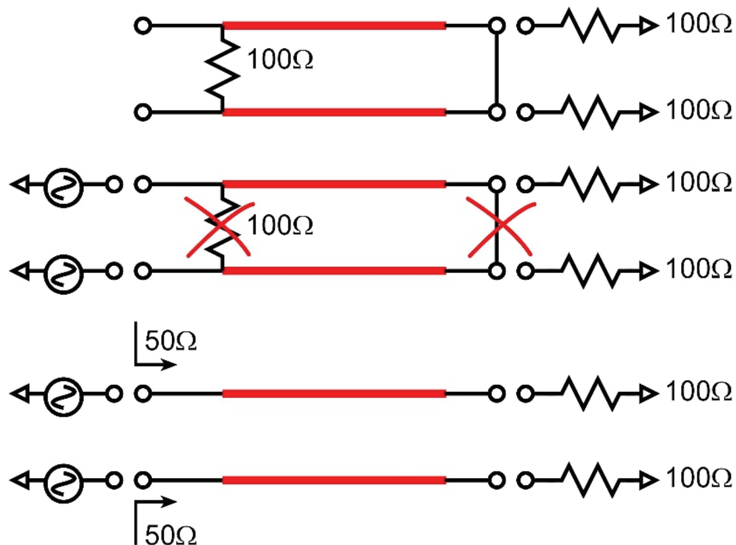
$50\Omega \cdot 2^{-1/2} = 35.4\Omega$

$50\Omega/2 = 25\Omega$

Even-mode (in-phase) inputs

$Z_{in} = Z_0$

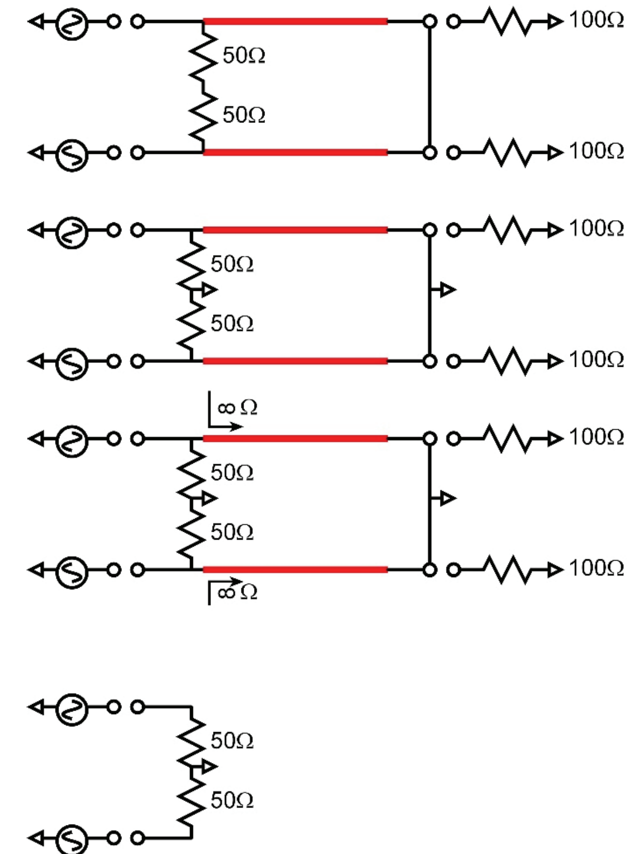
Power from each input goes to the output



odd-mode (out-of-phase) inputs

$Z_{in} = Z_0$

100% of P_{in} goes to bridge resistor



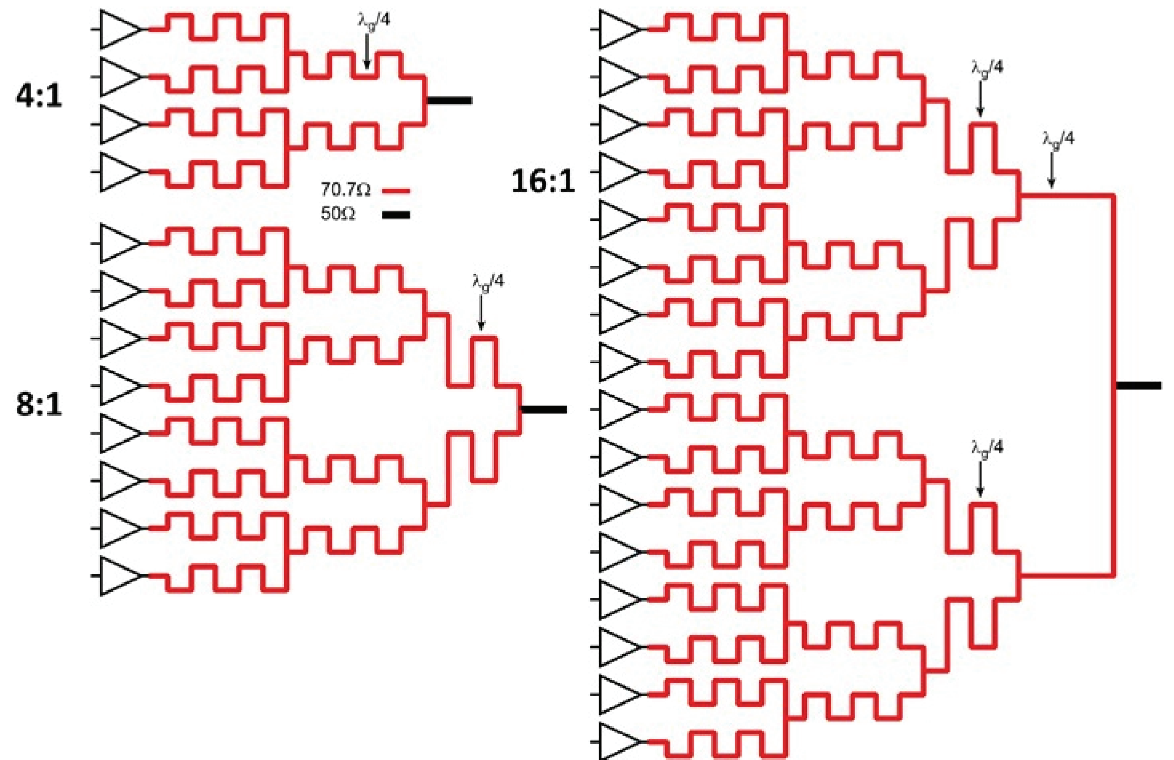
If we are confident that there will be no odd-mode, we can remove the bridge resistor.

Corporate Wilkinson Power-combiner

Requires inductive pre-tuning

Assume: all these lines are $\sqrt{2}\times 50\Omega$ impedance
Assume: all these lines are quarter-wavelength.
Then: these are Wilkinson power-combiners
Provide 2^N:1 power-combining

Corporate Wilkinson combiners are *rare* in ICs. Why ?
Signal passes through several 71Ω, $\lambda/4$ lines.
$\lambda/4$ lines are very long.
71Ω lines are narrow and hence high loss per unit length.
Structure is large and uses much IC die area.



Losses of on-wafer microstrip line

Keysight/ADS/Linecalc formula-based calculations of line skin-effect loss

Recollect line loss analysis from ECE145A/218A

Assumed geometry (lines on InP HBT IC)
insulator: benzocyclobutene (BCB)
6μm thick
$\varepsilon_r = 2.65$
conductors: gold, 200 nm thick

Line losses on Si CMOS IC will be similar:
similar insulator thickness, slightly higher ε_r.
slightly more conductive (Cu) conductors

Simulations neglect radiation losses
(so actual losses are somewhat greater)

LineCalc/untitled
File Simulation Options Help
Component: Type MLIN, ID MLIN: TL20
Substrate Parameters: ID MSub1; H 6.000 um; Er 2.650; Mur 1.000; Cond 4.1E7; Hu 1e+36 um; T 0.200 um; TanD 0.000
Component Parameters: Freq 210.000 GHz; Wall1 1.0E+30 um; Wall2 1.0E+30 um
Physical: W 42.024300 um; L 233.318000 um
Synthesize / Analyze
Electrical: Z0 25.000 Ohm; E_Eff 90.000 deg
Calculated Results: K_Eff = 2.339; A_DB = 0.137; SkinDepth = 0.006
Values are consistent

Substrate Parameters: ID MSub1; H 6.000 um; Er 2.650; Mur 1.000; Cond 4.1E7; Hu 1e+36 um; T 0.200 um; TanD 0.000
Component Parameters: Freq 210.000 GHz; Wall1 1.0E+30 um; Wall2 1.0E+30 um
Physical: W 26.687200 um; L 237.242000 um
Electrical: Z0 35.350 Ohm; E_Eff 90.000 deg
Calculated Results: K_Eff = 2.263; A_DB = 0.156; SkinDepth = 0.006
Values are consistent

Substrate Parameters: ID MSub1; H 6.000 um; Er 2.650; Mur 1.000; Cond 4.1E7; Hu 1e+36 um; T 0.200 um; TanD 0.000
Component Parameters: Freq 210.000 GHz; Wall1 1.0E+30 um; Wall2 1.0E+30 um
Physical: W 16.111300 um; L 241.766000 um
Electrical: Z0 50.000 Ohm; E_Eff 90.000 deg
Calculated Results: K_Eff = 2.179; A_DB = 0.186; SkinDepth = 0.006
Values are consistent

On-Wafer Interconnect Losses

Interconnects in packages and on PCBs:

$H \propto 1/\text{frequency}$ (to control radiation loss)

$\text{loss (dB/mm)} \propto (\text{frequency})^{3/2}$

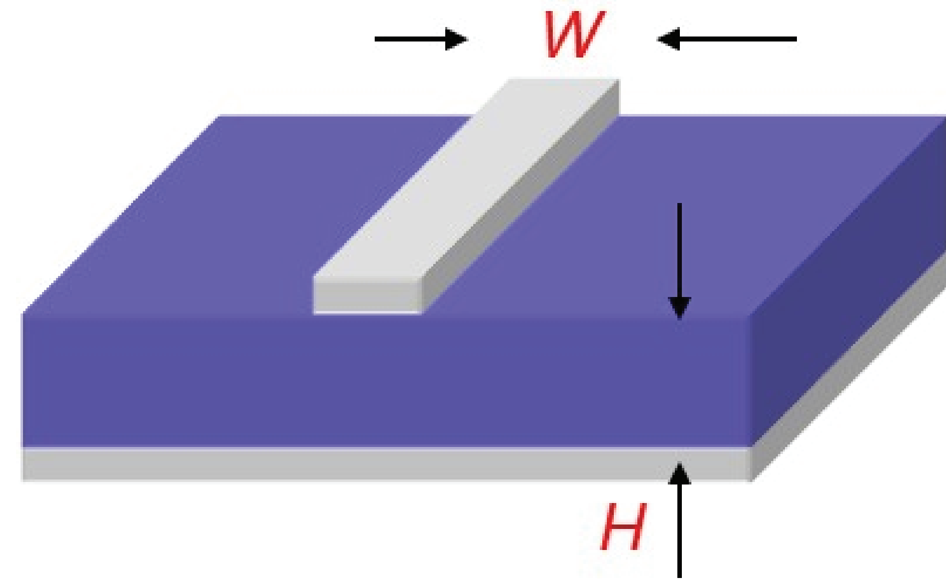
$\text{loss (dB/wavelength)} \propto \sqrt{\text{frequency}}$

Interconnects in ICs:

H is independent of frequency

$\text{loss (dB/mm)} \propto \sqrt{\text{frequency}}$

$\text{loss (dB/wavelength)} \propto 1/\sqrt{\text{frequency}}$



Losses on a quarter-wave impedance transformer

On a transmission-line:

$$V(z,t)=V^{+}(z)e^{j\omega t}+V^{-}(z)e^{j\omega t}=V^{+}(0)e^{j\omega t}e^{-j\beta z}e^{-\alpha z}+V^{-}(z)e^{j\omega t}e^{j\beta z}e^{\alpha z}$$

Note: $e^{-\alpha z}$ voltage attenuation, $e^{-2\alpha z}$ power attenuation

On a quarter-wave line:

$$Z_{line}=\sqrt{Z_{in}Z_{load}}\ ,\ \Gamma=\left((Z_{load}/Z_{line})-1\right)\Big/\left((Z_{load}/Z_{line})+1\right)$$

Forward and reverse waves: quarter-wave line losses are larger than single-pass ($e^{-2\alpha z}$) loss

We can show that:

$$\frac{P_{out}}{P_{in}}=\frac{\left(1-\|\Gamma\|^2\right)^2 e^{-2\alpha l}}{\left(1-e^{-2\alpha l}\|\Gamma\|^2\right)^2}=\frac{\left(1-\left\|\dfrac{\sqrt{Z_{load}/Z_{in}}-1}{\sqrt{Z_{load}/Z_{in}}+1}\right\|^2\right)^2 e^{-2\alpha l}}{\left(1-e^{-2\alpha l}\left\|\dfrac{\sqrt{Z_{load}/Z_{in}}-1}{\sqrt{Z_{load}/Z_{in}}+1}\right\|^2\right)^2}=\frac{\left(1-\left\|\dfrac{\sqrt{Z_{load}/Z_{in}}-1}{\sqrt{Z_{load}/Z_{in}}+1}\right\|^2\right)^2 e^{-2\alpha l}}{\left(1-e^{-2\alpha l}\left\|\dfrac{\sqrt{Z_{load}/Z_{in}}-1}{\sqrt{Z_{load}/Z_{in}}+1}\right\|^2\right)^2}$$

Quarter-wave line losses increase with increased impedance transformation ratio

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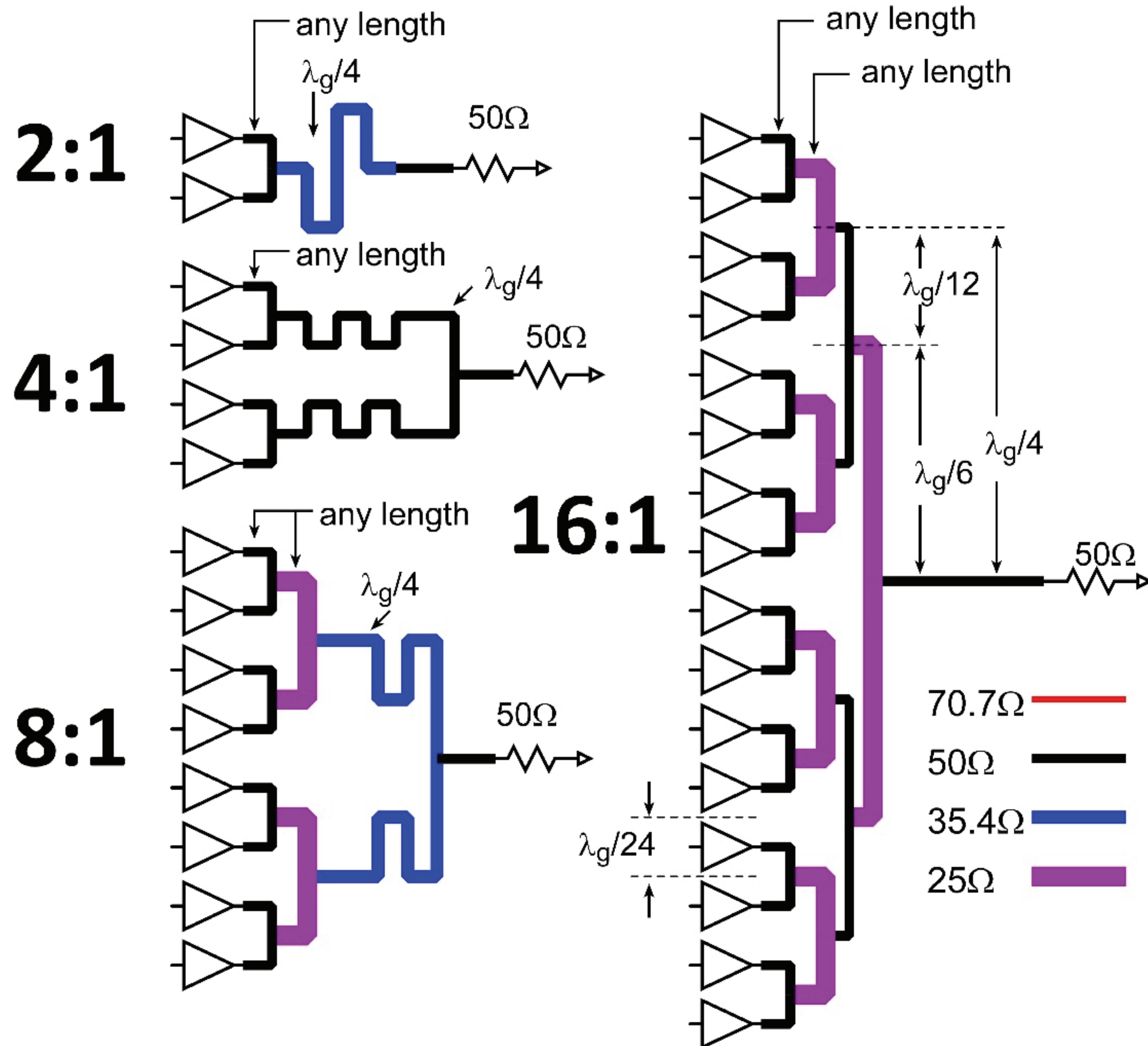
Low-Loss Corporate Combiners (Inductively-pretuned)

Single-(λ/4) combiners are much less lossy
Each design uses a single *effective* λ/4 section.
Shorter lines, low-Z_o lines → lower loss
But, low loss only if transistor cells fit.

...if they don't fit, then the non- λ/4 lines must be made longer, and losses will increase.

$50\Omega \cdot 2^{1/2} = 70.7\Omega$
50Ω
$50\Omega \cdot 2^{-1/2} = 35.4\Omega$
$50\Omega/2 = 25\Omega$



Low-Loss Corporate Combiners: Analysis

$\lambda_g/4$

50Ω

$\lambda_g/4$

100Ω

100Ω

$Z_{in}=(35.4\Omega)^2/100\Omega$
$=12.5\Omega$

$\lambda_g/4$

100Ω

$Z_{in}=(35.4\Omega)^2/100\Omega$
$=12.5\Omega$

100Ω

12.5Ω

12.5Ω

25Ω

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$50\Omega\cdot 2^{1/2} = 70.7\Omega$

50Ω

$50\Omega\cdot 2^{-1/2} = 35.4\Omega$

$50\Omega/2 = 25\Omega$

Low-Loss Corporate Combiners: Analysis

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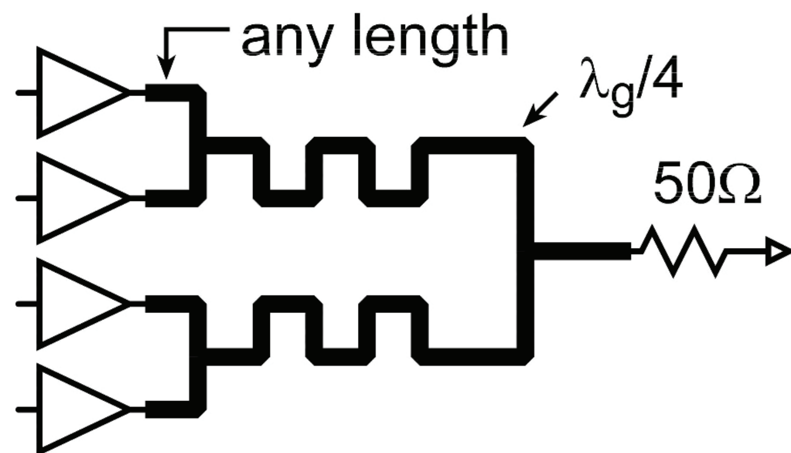
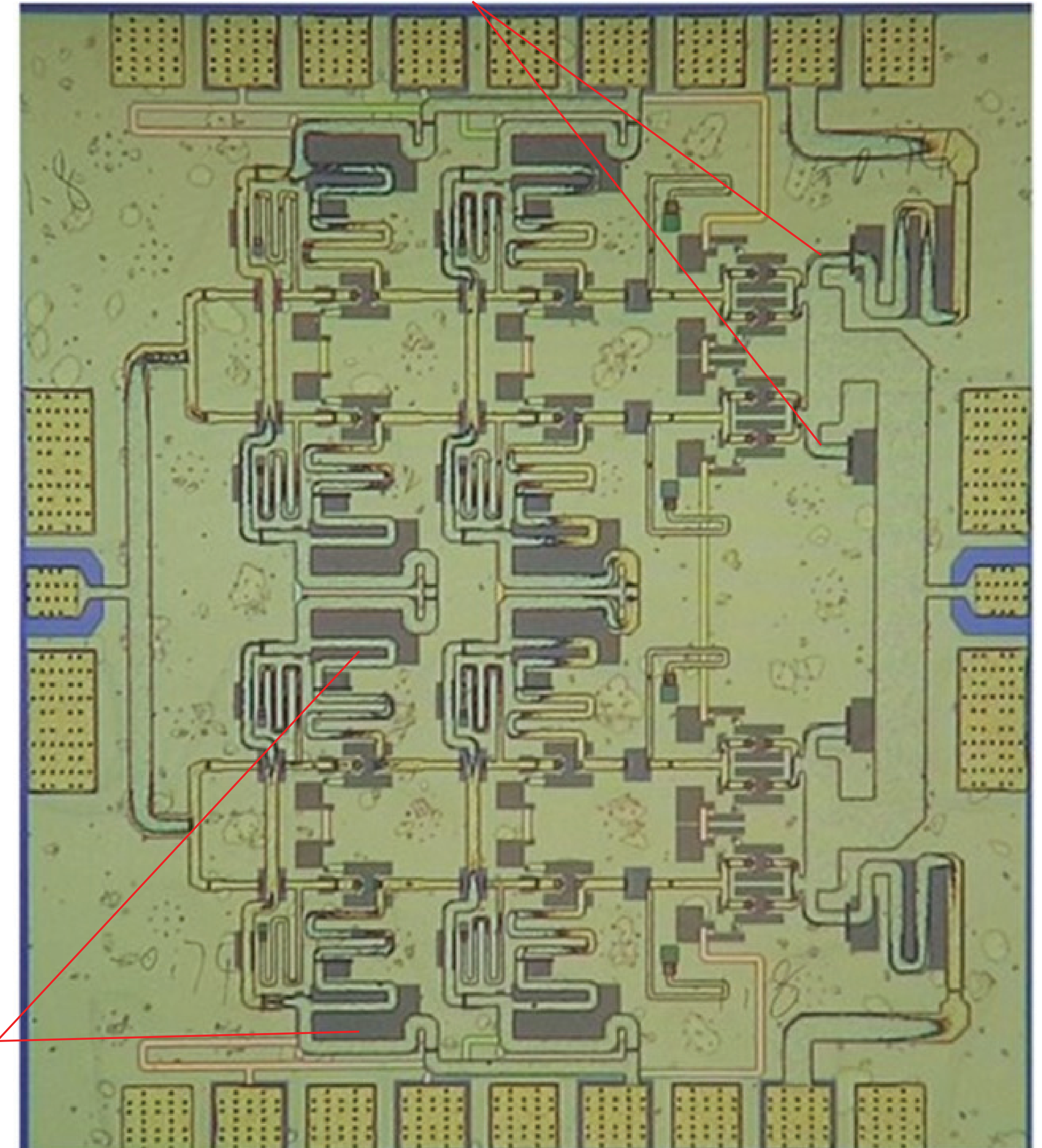
Design example (200 GHz PA)

The *first pass* of the IC power-combining network was designed using the idealized 4:1 network shown.

Line parameters were subsequently adjusted to accommodate probe parasitics, etc.

Note the uncontrolled-impedance lines within the multi-finger transistor cells (these almost too small to see)



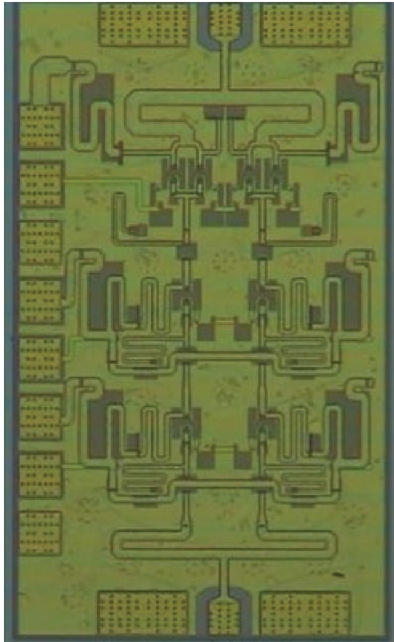


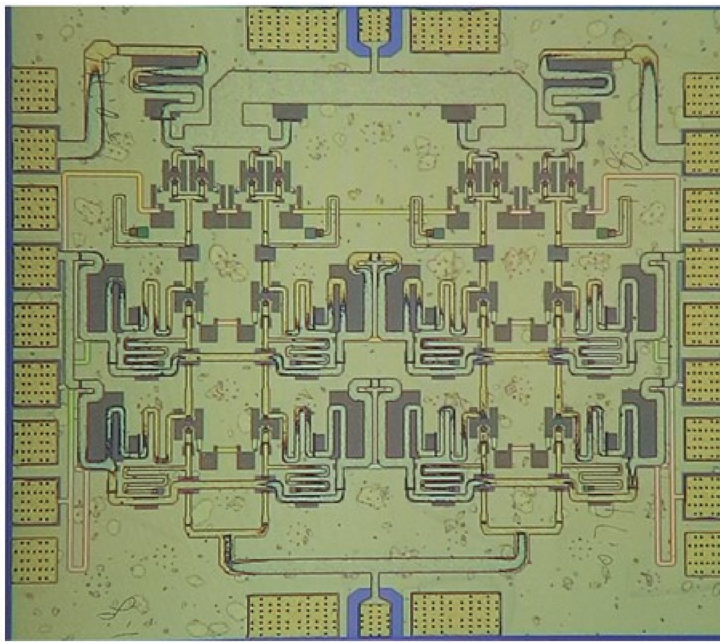
Ahmed et al, 2020 IMS: 200 GHz PA in 250 nm InP HBT

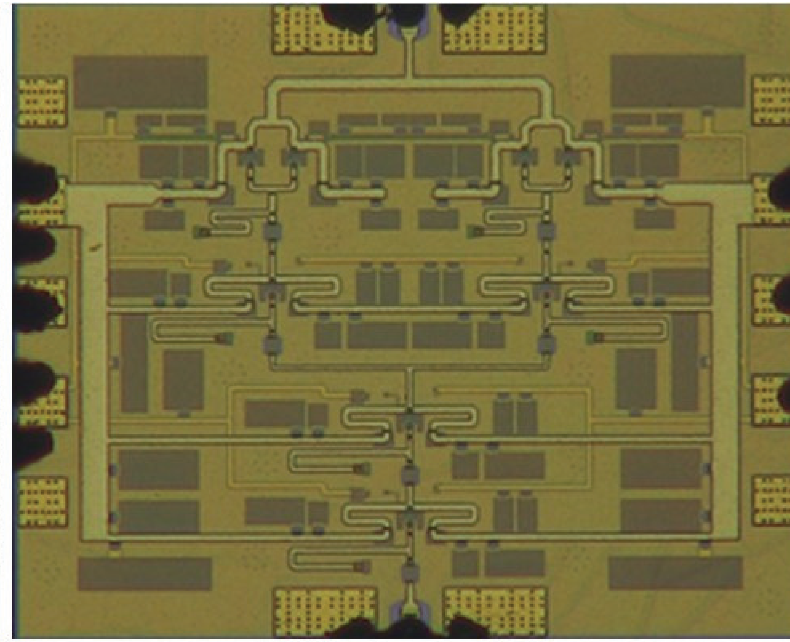
PAs with corporate & cascade combining

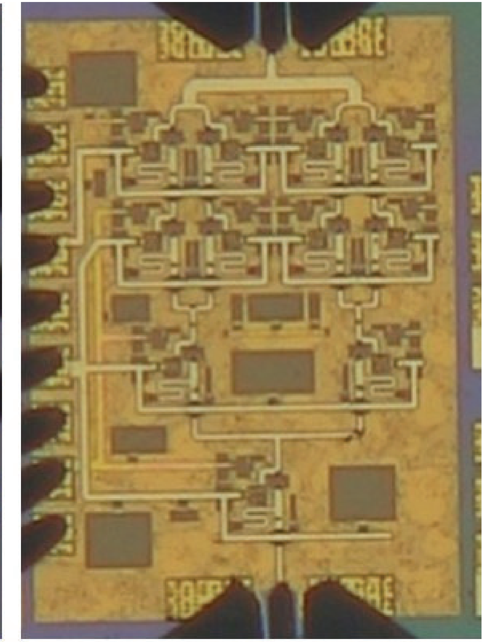
Teledyne 250nm InP HBT technology

Ahmed et al., 2020 IMS, 2020 EuMIC, 2021 IMS, 2021 RFIC







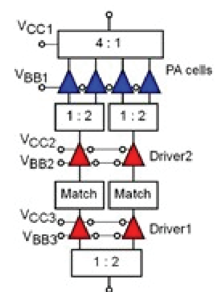


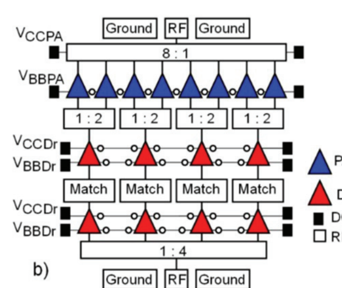
140GHz, 20.5dBm, 20.8% PAE

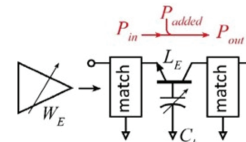
130GHz, 200mW, 17.8% PAE

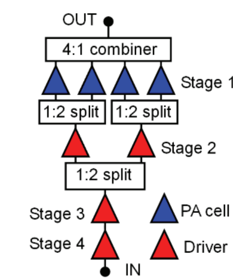
194GHz, 17.4dBm, 8.5% PAE

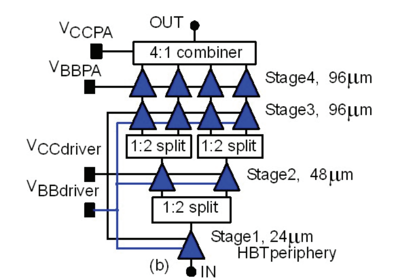
266GHz, 16.8dBm, 4.0% PAE











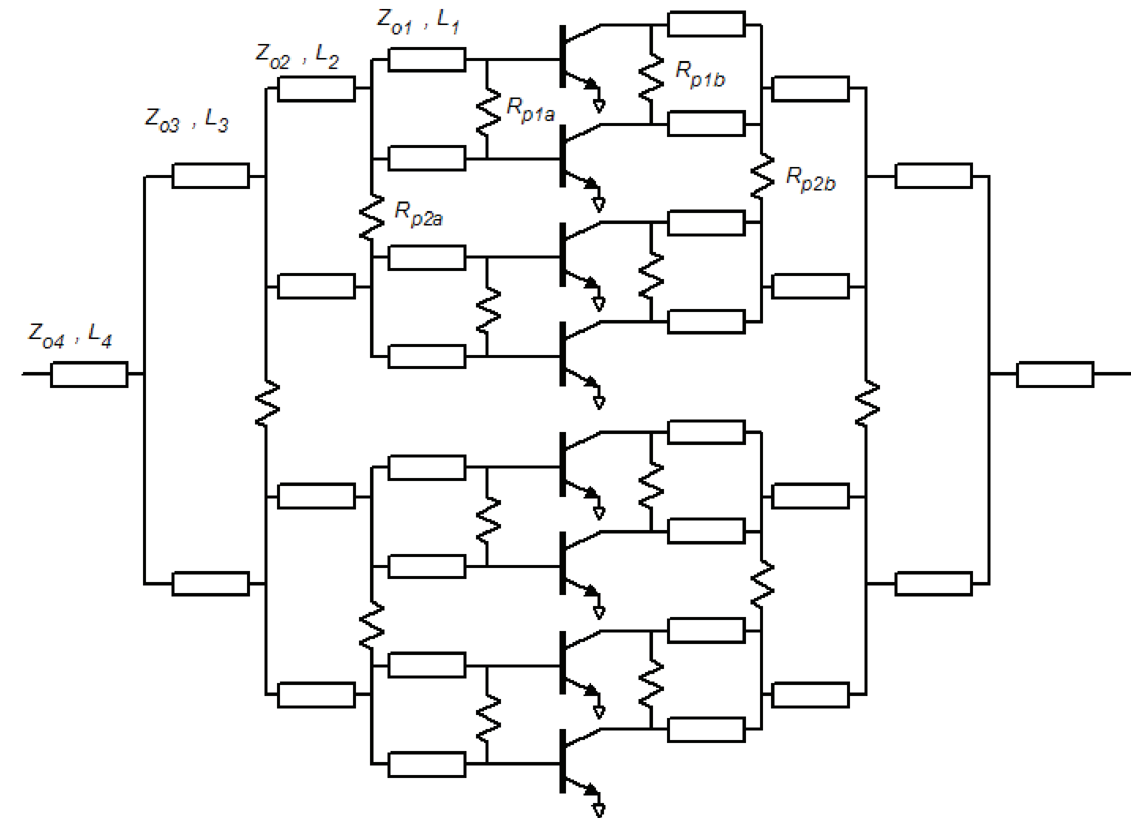
Design of Non-Wilkinson Combiners

The equivalent circuit:
a multi-section transmission-line tuning network

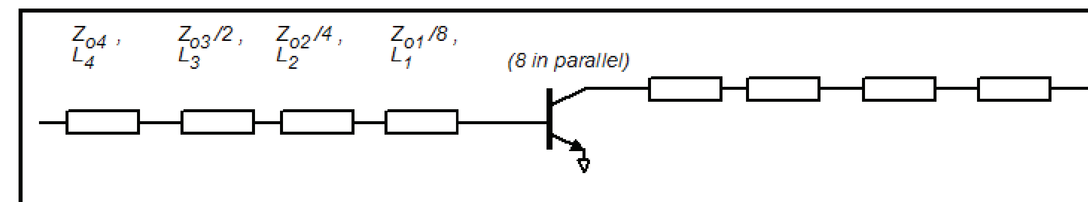
Shunt elements (inductive lines, capacitors)
can also be added.

Line parameters are adjusted to reach $Z_{l,opt}$.

CAD approach:
all similar lines defined by shared variables,
simultaneously adjusted



Even-mode equivalent circuit



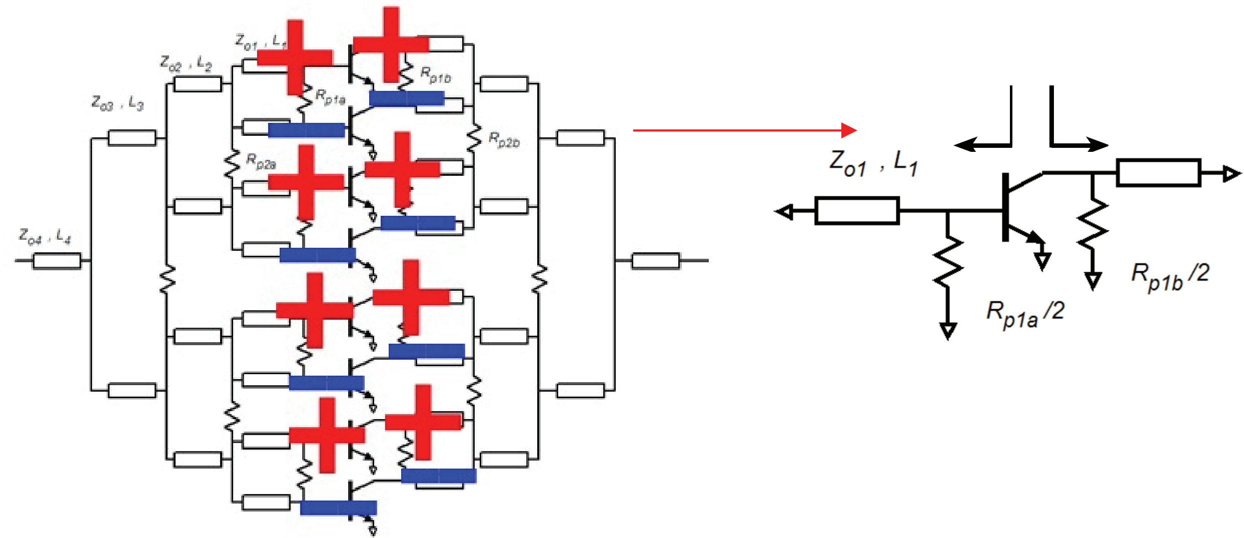
Design: Multi-Finger Amplifiers: spatial mode instabilities

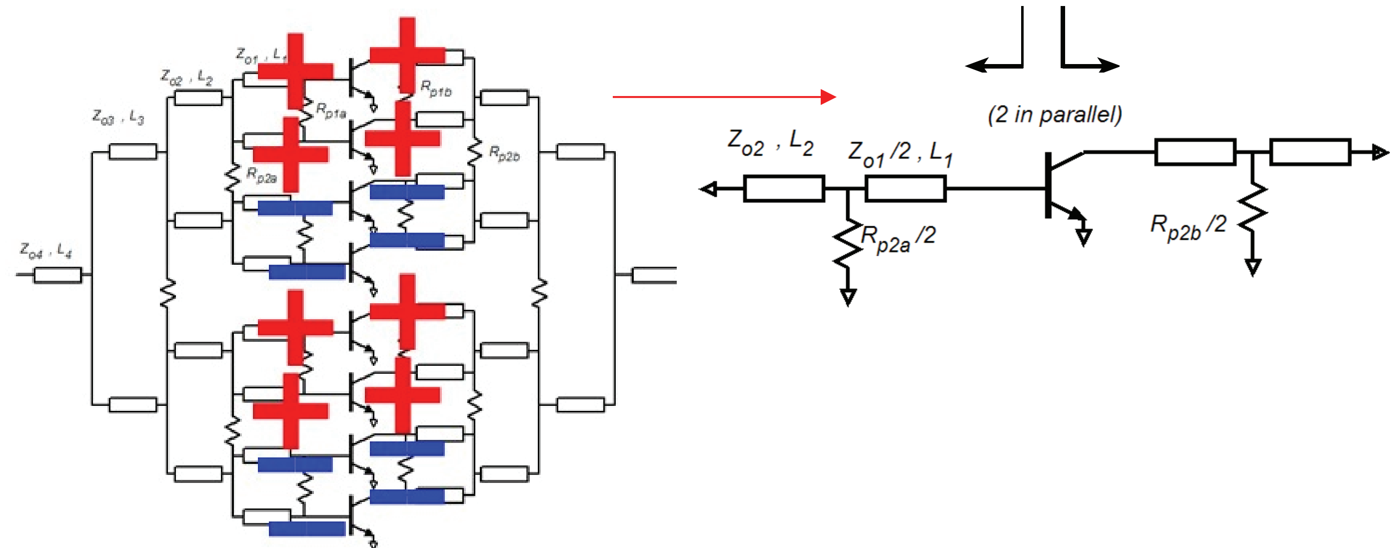
If each transistor finger is individually stabilized, high-order modes are stable.

Amplifier layout does not always allow sufficient space for this.

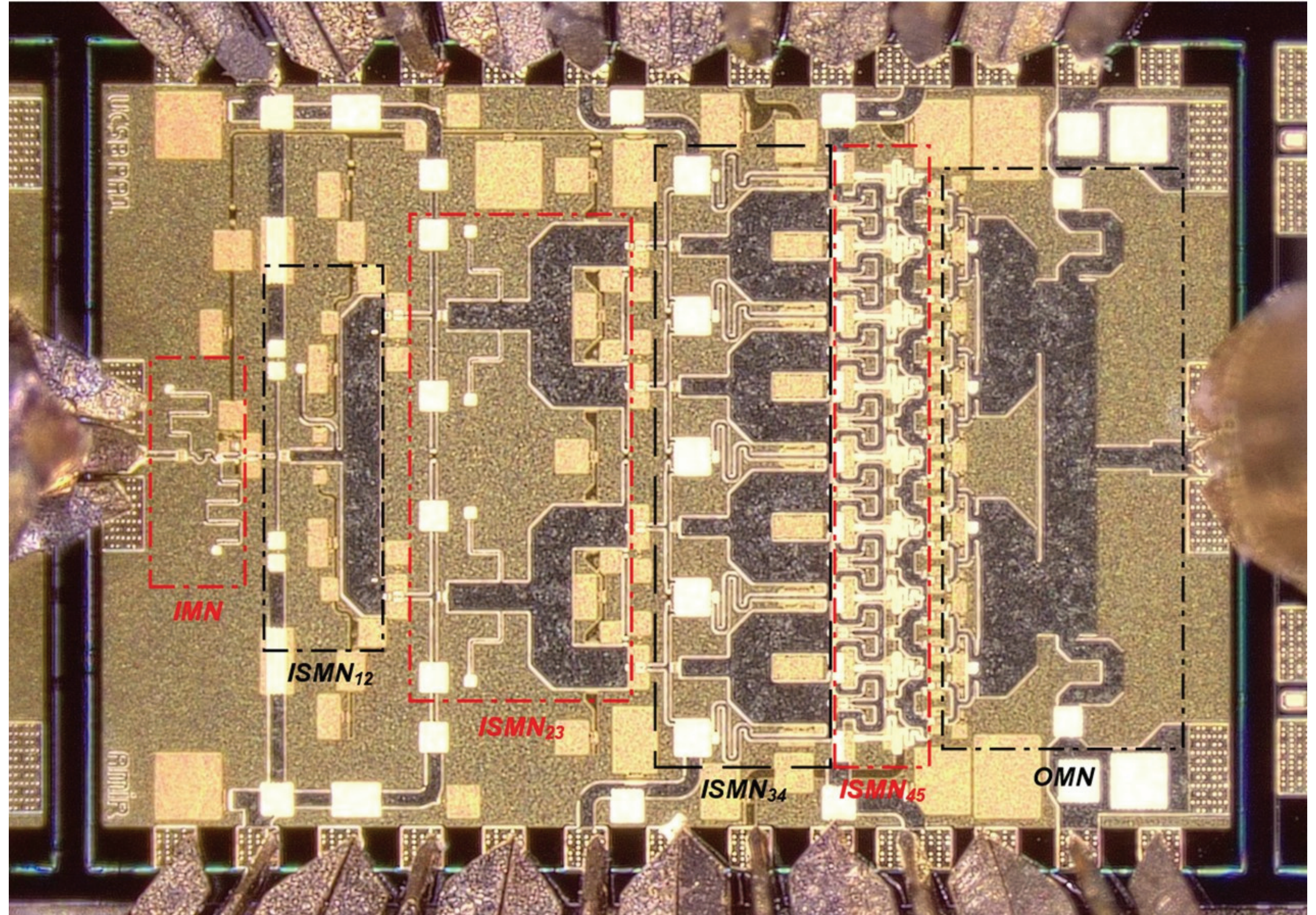
All spatial modes must then be stabilized.

Stabilization method: bridging resistors parallel loading of higher-order modes selected such that (Z_S, Z_L) presented to device lie in the stable regions





Combiner without inductive pre-tuning.



Alizadeh et al, 2023 BCICTS

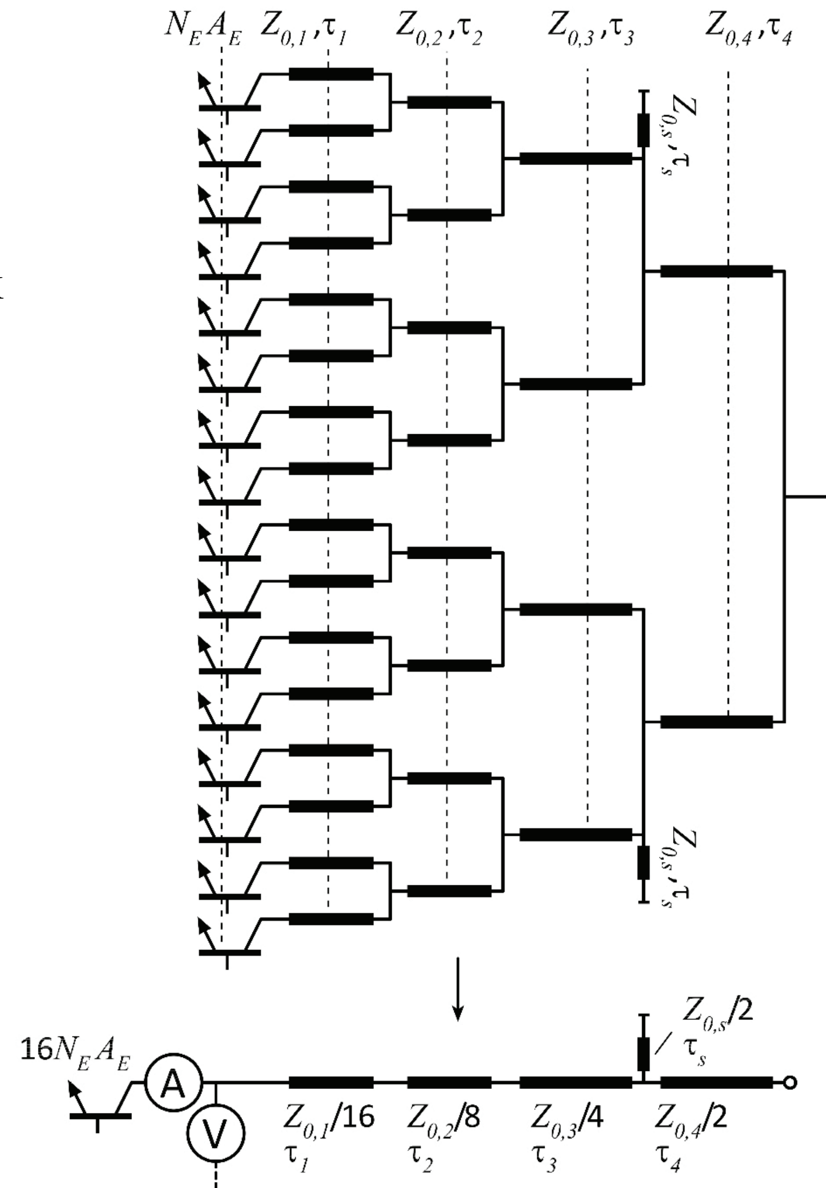
Combiner without inductive pre-tuning.

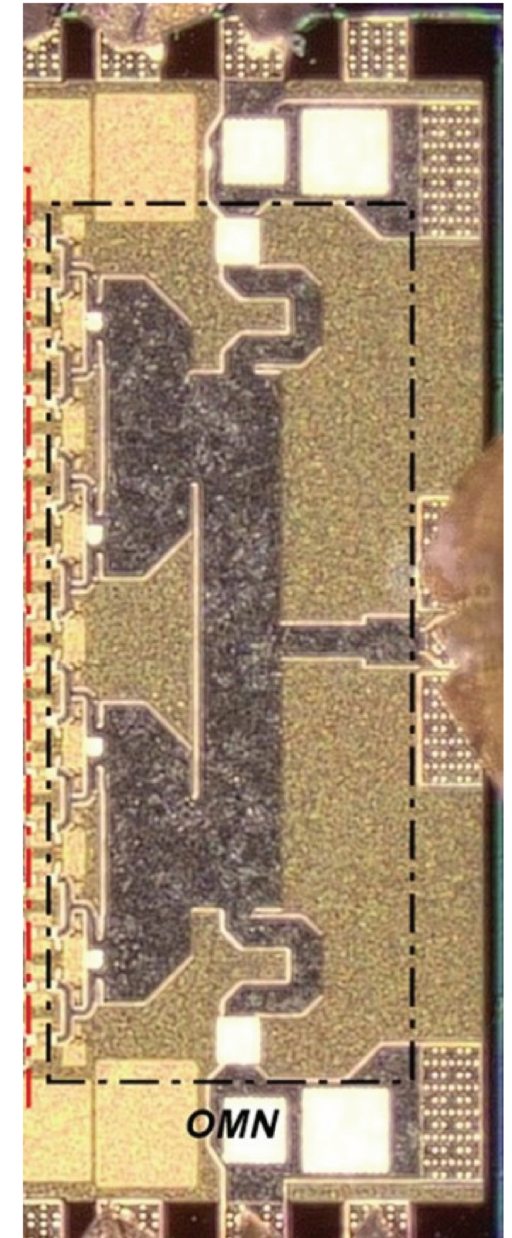
Again:

The equivalent circuit:
a multi-section transmission-line tuning network

Shunt elements (inductive lines, capacitors)
can also be added.

Line parameters are adjusted to reach $Z_{l,opt}$.

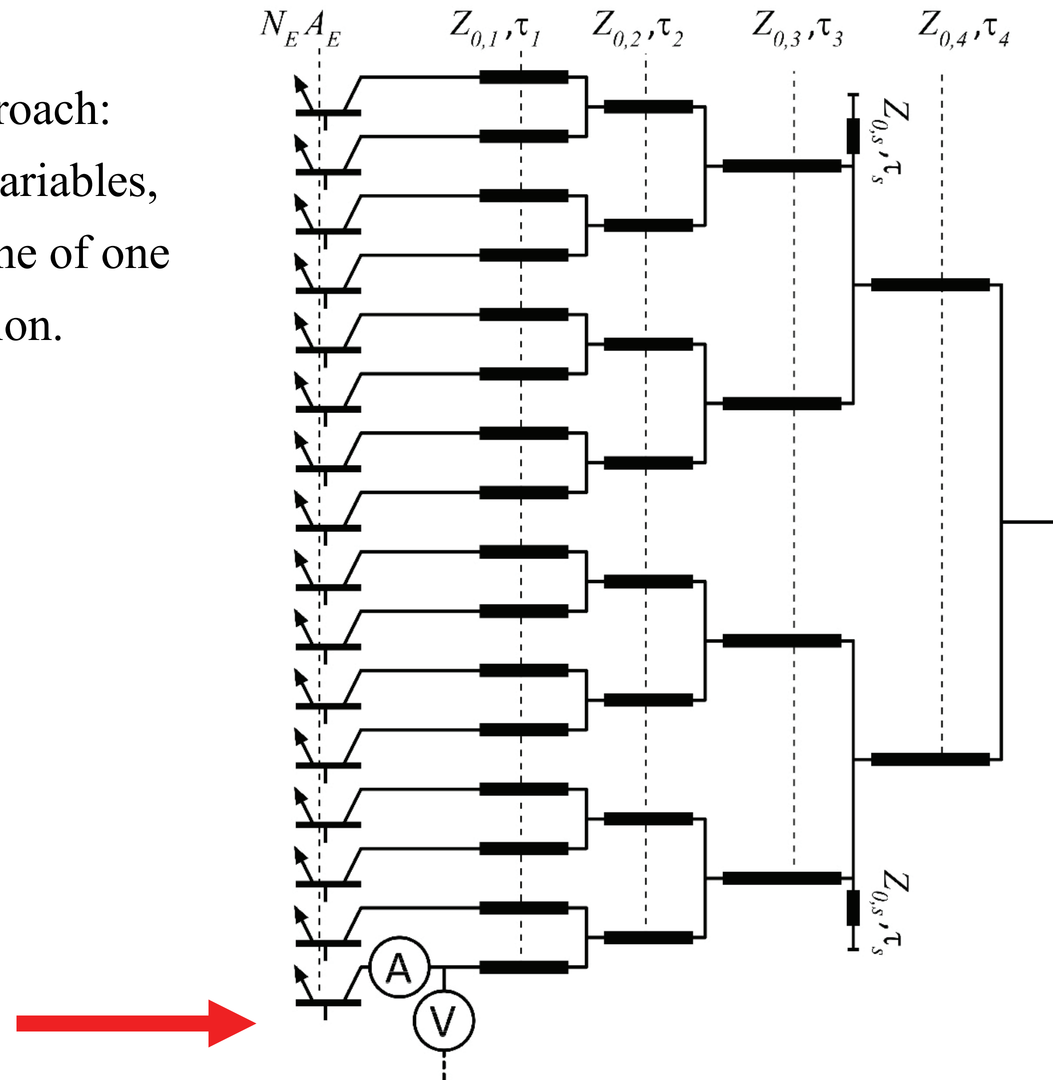


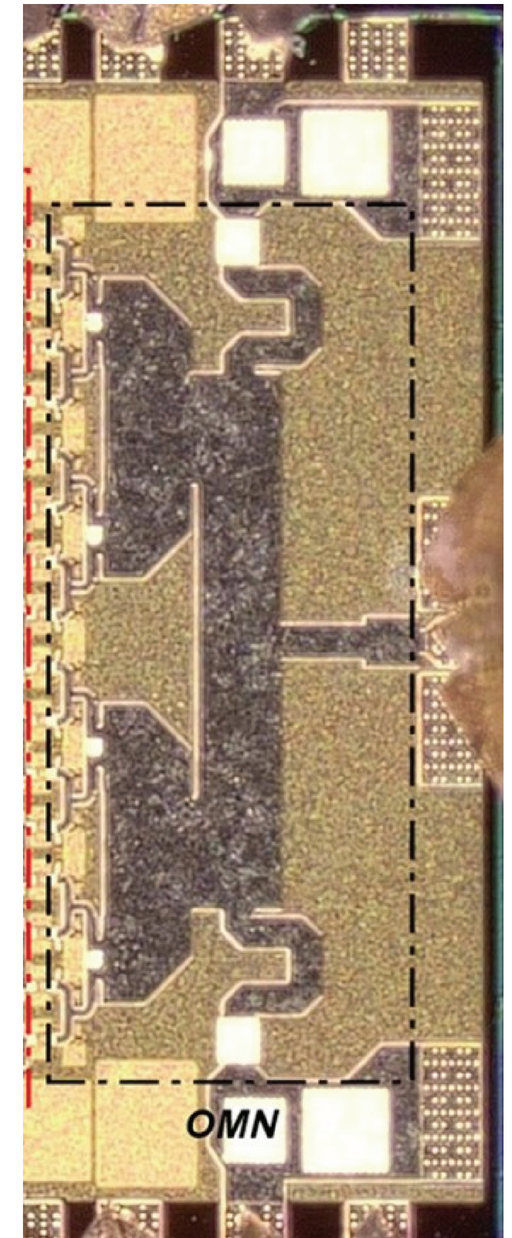


Alizadeh et al, 2023 BCICTS

Combiner without inductive pre-tuning.

Computer-aided design (CAD) approach:
all similar lines defined by shared variables, simultaneously adjusted, and loadline of one transistor cell monitored in simulation.





Alizadeh et al, 2023 BCICTS

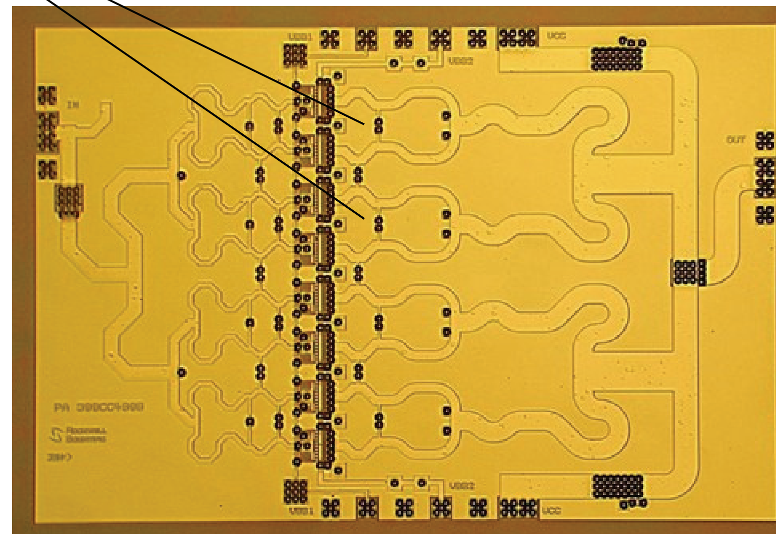
Examples: PAs with corporate combining

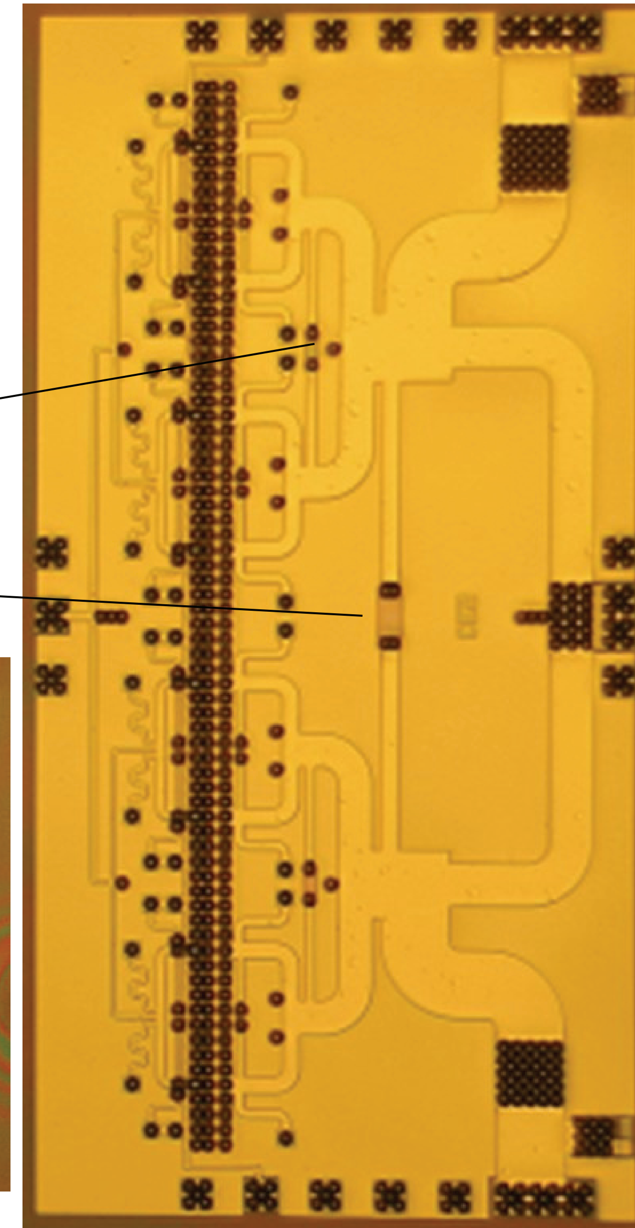
34 GHz InP HBT power amplfiers

Design: Jonathan Hacker, Teledyne
(at the time, Rockwell Scientific)

Power combiners without inductive pre-tuning

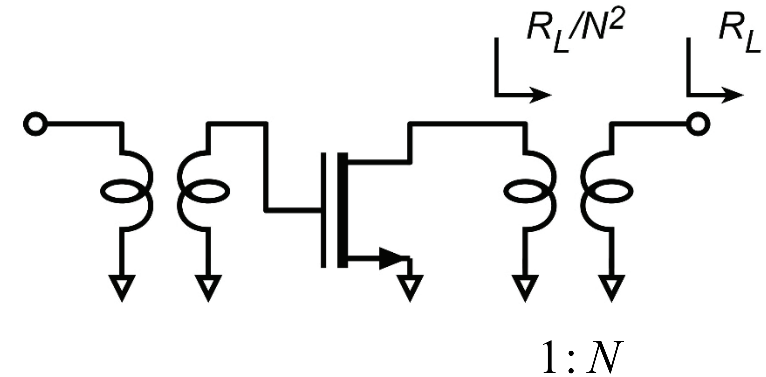
Bridging resistors for odd mode stabilization.





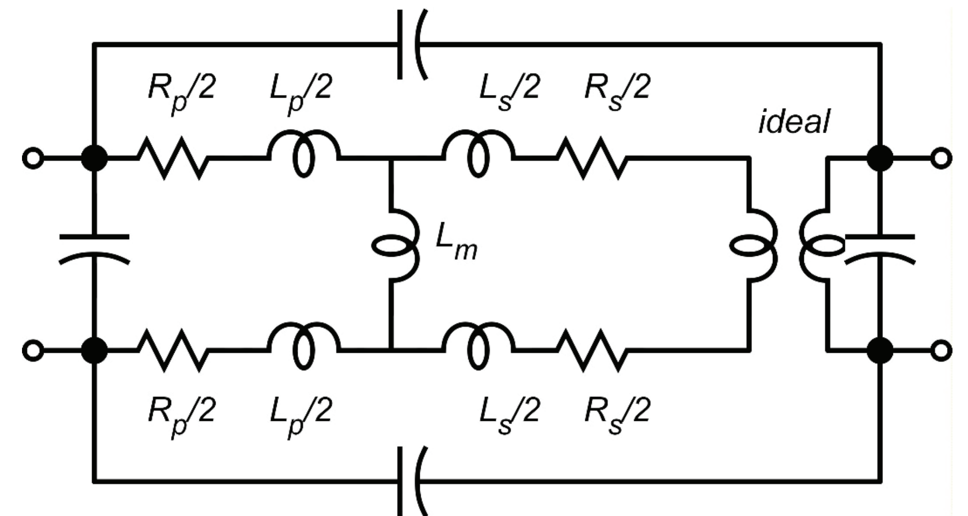
Transformers for impedance transformation

Here the transformer changes (decreases) the real part of the load admittance.



Additional tuning elements used to adjust $\text{Im}(Y_L)$

Transformers have extensive parastics and require careful electromagnetic modeling



class notes, M. Rodwell, copyrighted 2012-2024

Transformers for power combining

With ideal transformers:

$V_p = V_o/2$

$I_P = I_o = V_o / R_L = 2V_P / R_L$

$\rightarrow V_P / I_P = R_L / 2$

1) Each PA is loaded in $R_L / 2$, not R_L

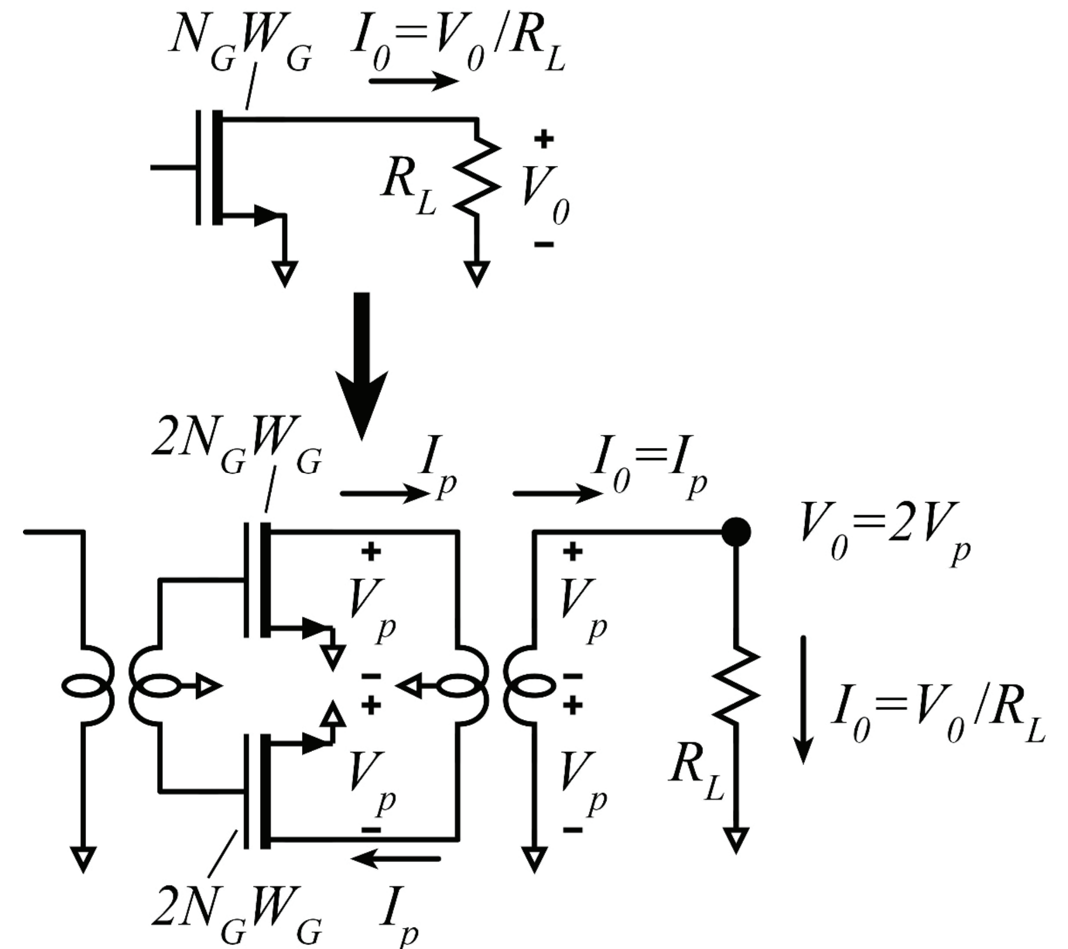
Can use 2:1 larger $N_g W_g$ or 2:1 larger $N_E L_E$

$\rightarrow$ 2 : 1 larger output power for *each* element

2) Total output power from 2 PA cells

$\rightarrow$ 4:1 net increase in P_{out}

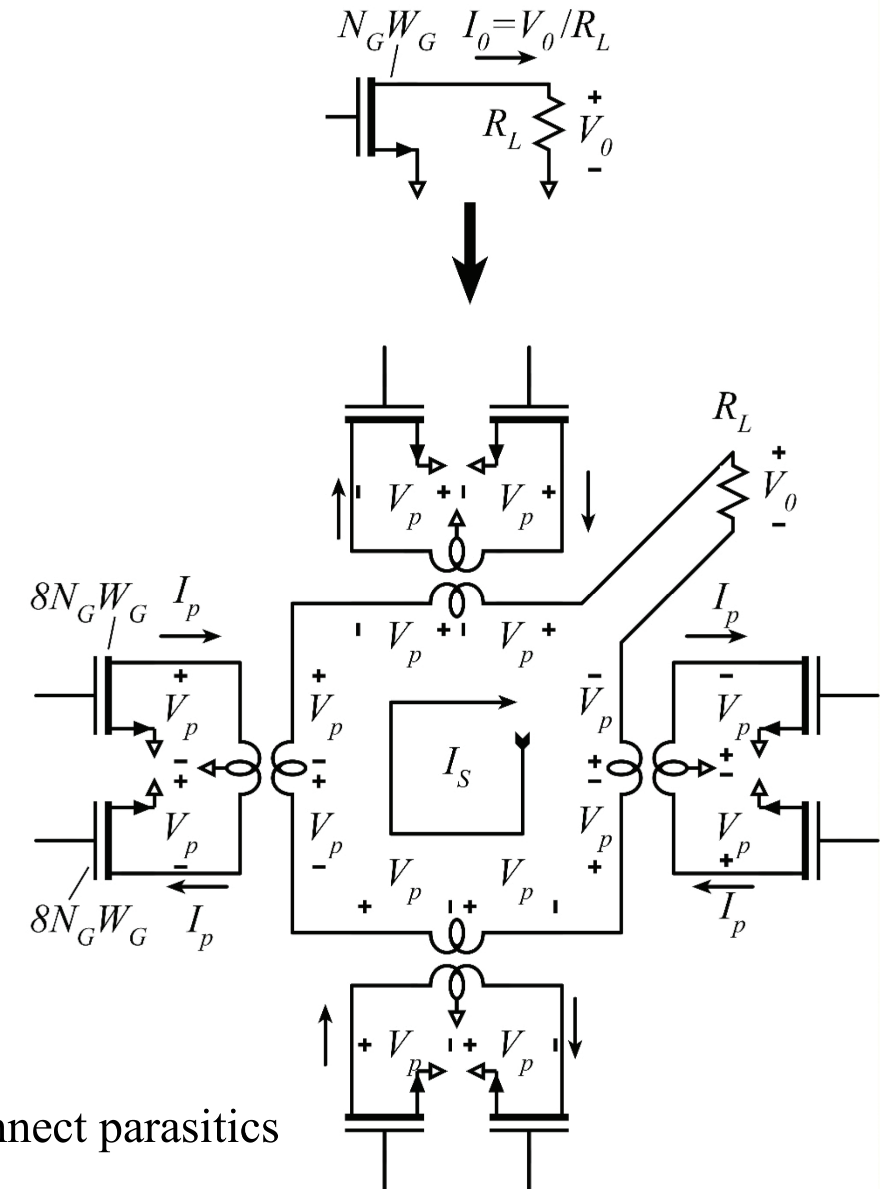
even with 1:1 transformer turns ratio



Transformers for power combining

I. Aoki *et al.* IEEE JSSC,March 2002

The transformer primary is segmented into 8 separate sub-windings.



With ideal transformers:

$V_p = V_o/8$

$I_P = I_o = V_o / R_L = 8V_P / R_L$

$\rightarrow V_P / I_P = R_L / 8$

1) Each PA is loaded in $R_L / 8$, not R_L

Can use 8:1 larger $N_g W_g$ or 8:1 larger $N_E L_E$

$\rightarrow 8:1$ larger output power for *each* element

2) Total output power from 8 PA cells

$\rightarrow$ 64:1 net increase in P_{out}

even with 1:1 transformer turns ratio

Limits to technique: real vs. ideal transformers. Very low $(R_L / 8) \rightarrow$ interconnect parasitics

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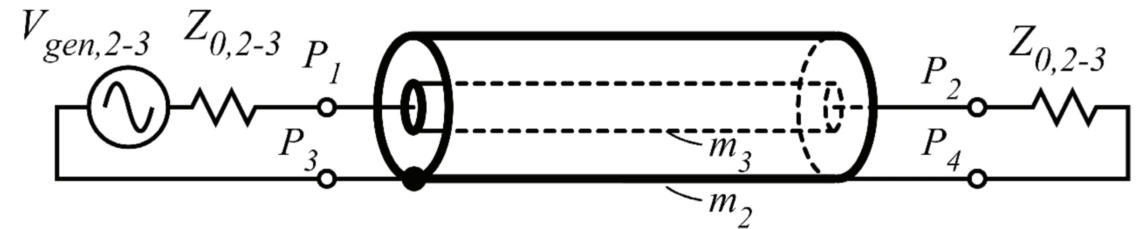
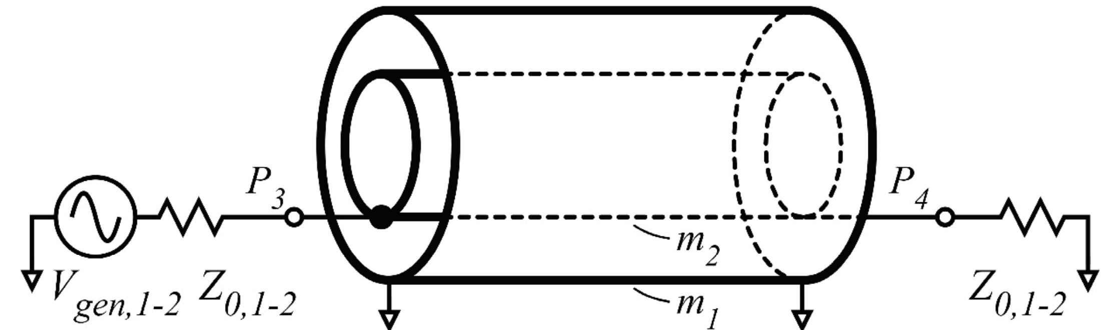
3-conductor transmission Lines: series-connected lines

Coaxial transmission-line between m_2 and m_3
characteristic impedance $Z_{0,2-3}$

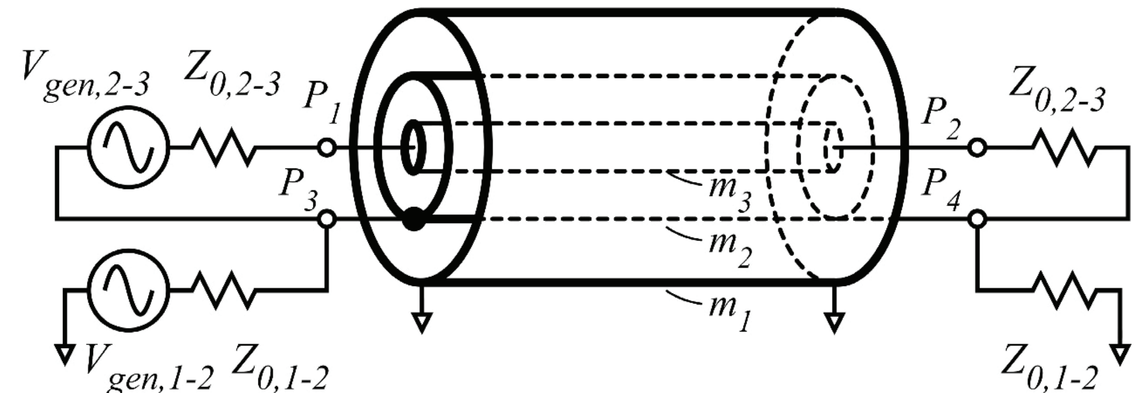


Coaxial transmission-line between m_1 and m_2
characteristic impedance $Z_{0,1-2}$



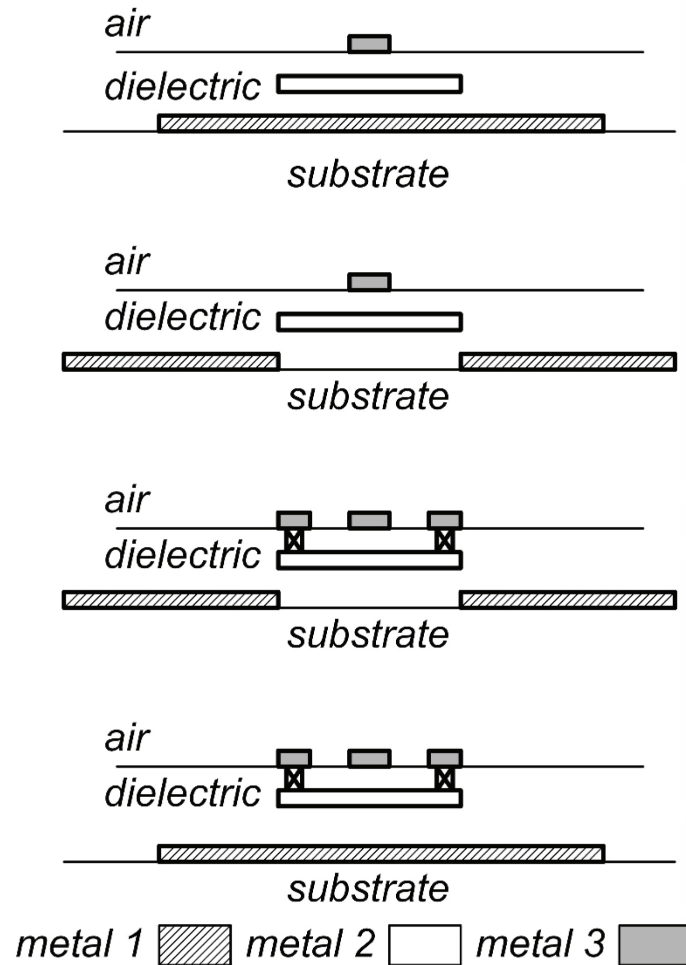
Both !
V_{gen1-2} launches input voltage wave on (m_1, m_2) transmission-line
V_{gen2-3} launches input voltage wave on (m_2, m_3) transmission-line

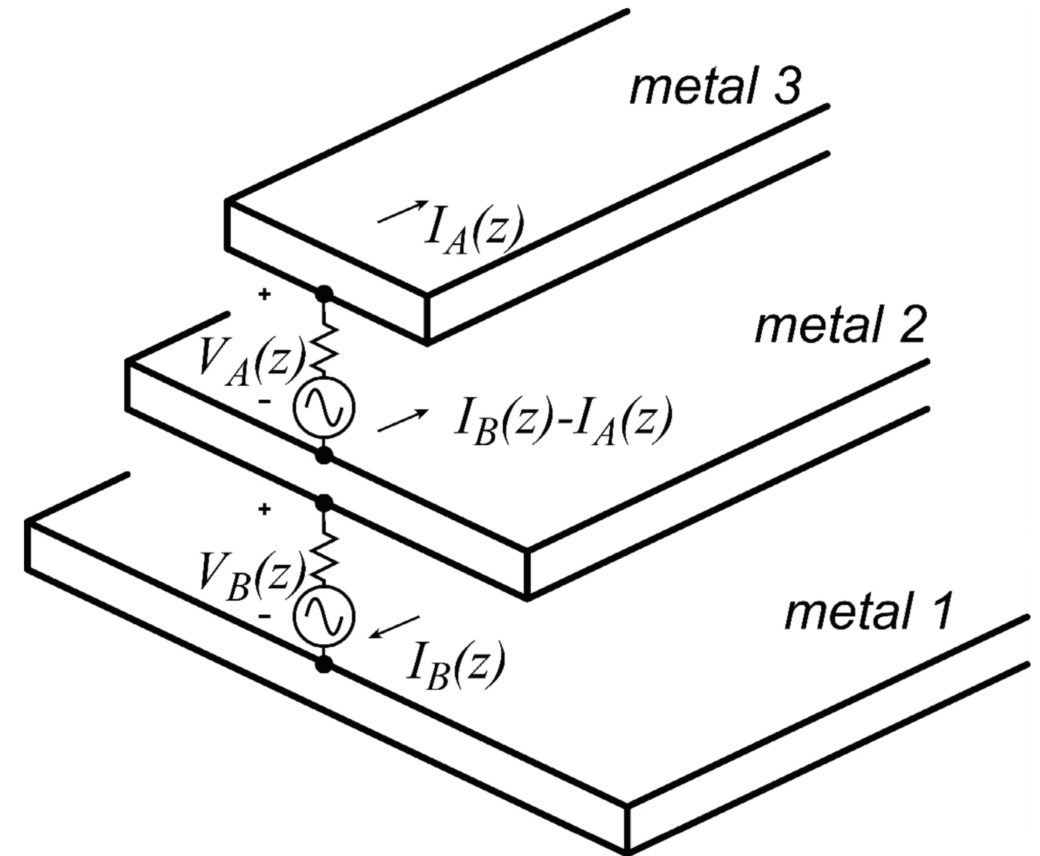
These transmission-lines are in *series*



Other 3-conductor transmission Line Geometries

These more suitable for IC implementations



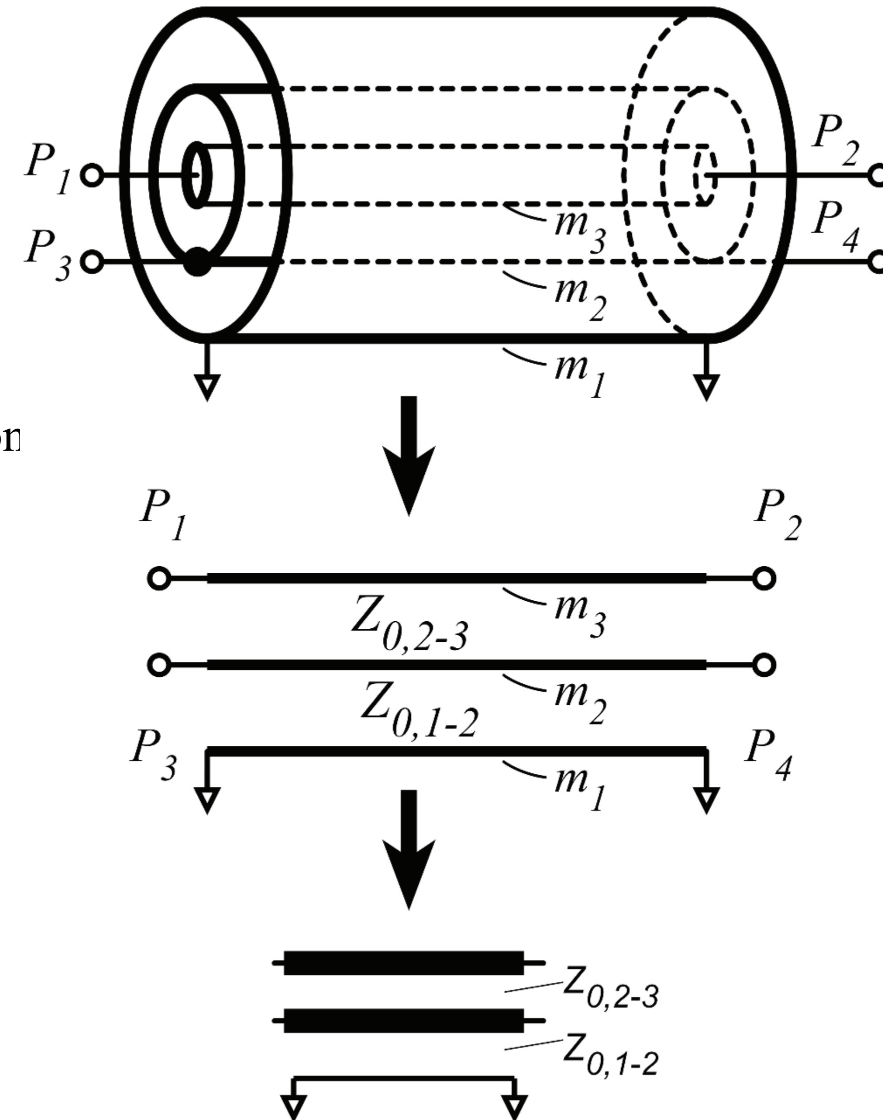


3-Conductor Line Circuit Symbol

We need a circuit symbol that is easier to draw.

...but if you are having trouble visualizing 3-conductor-line operation

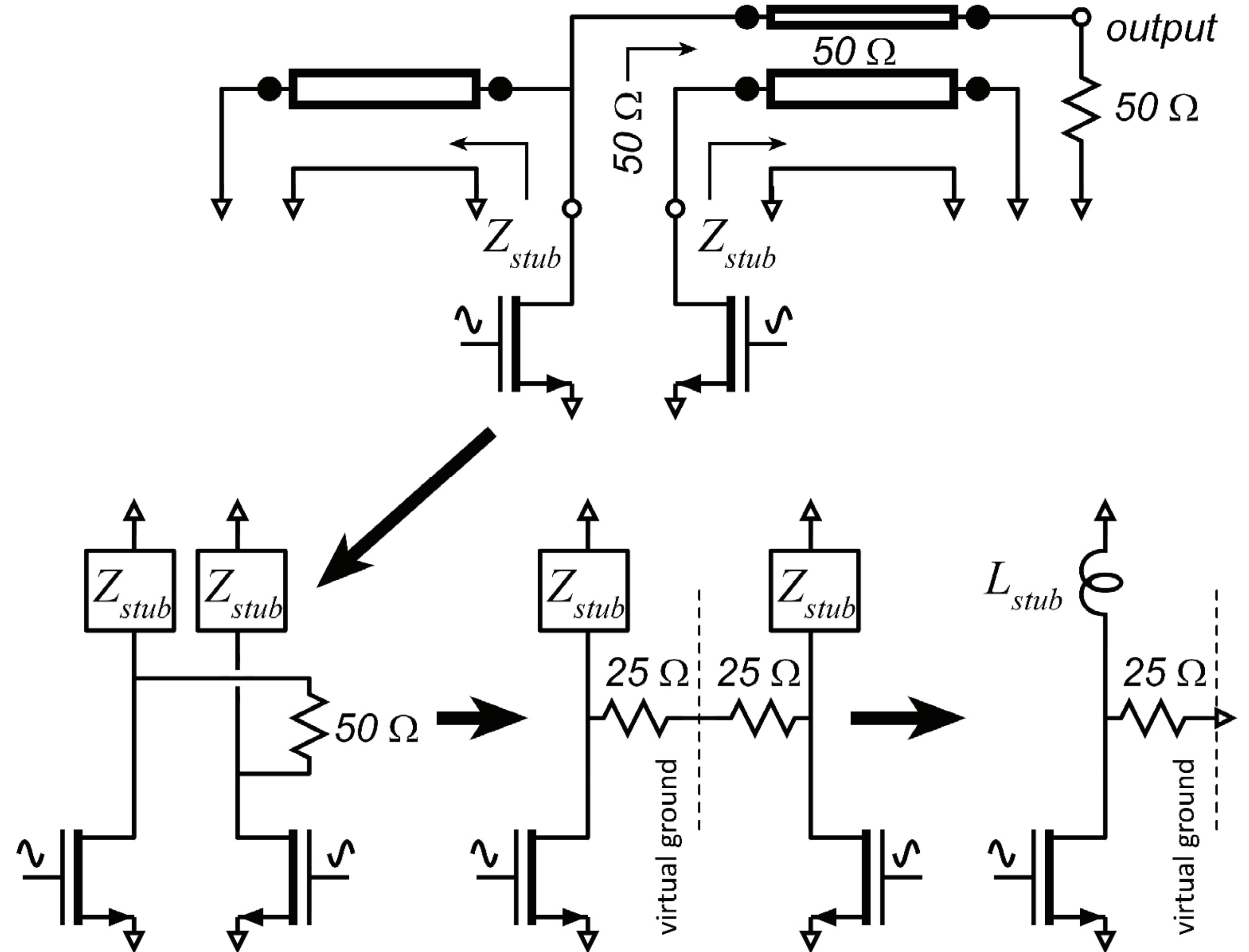
...go back to drawing them as coaxial cables.



Balun Power Combiner

As with the transformer design,
each transistor is loaded in 25Ω
$\rightarrow$ 2:1 greater $N_g W_g$ than FET that would drive 50Ω
$\rightarrow$ 2:1 greater P_{out} than FET that would drive 50Ω

2 such FETs.
$\rightarrow$ 4:1 greater P_{out} than FET that would drive 50Ω

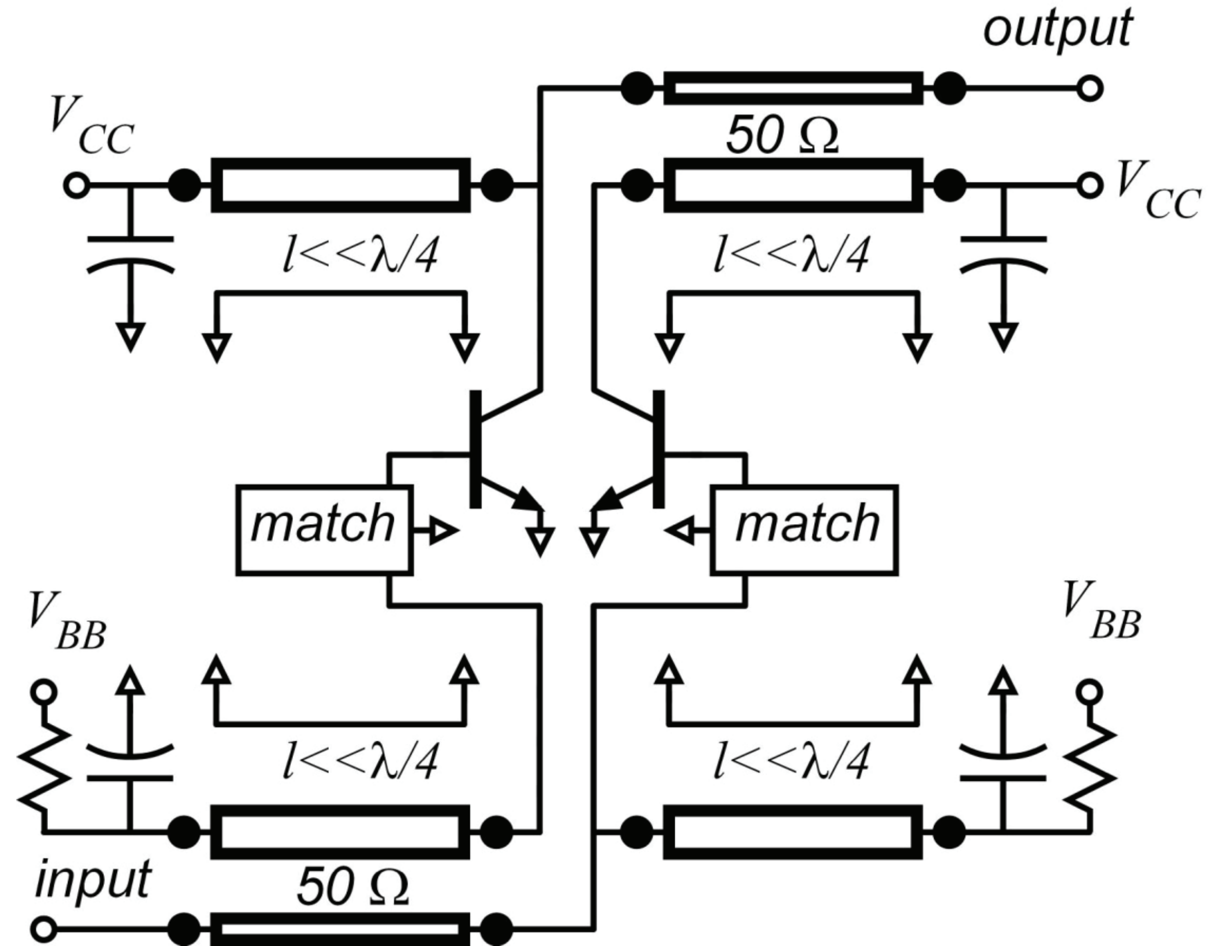


Amplifier with 2:1 balun combiners

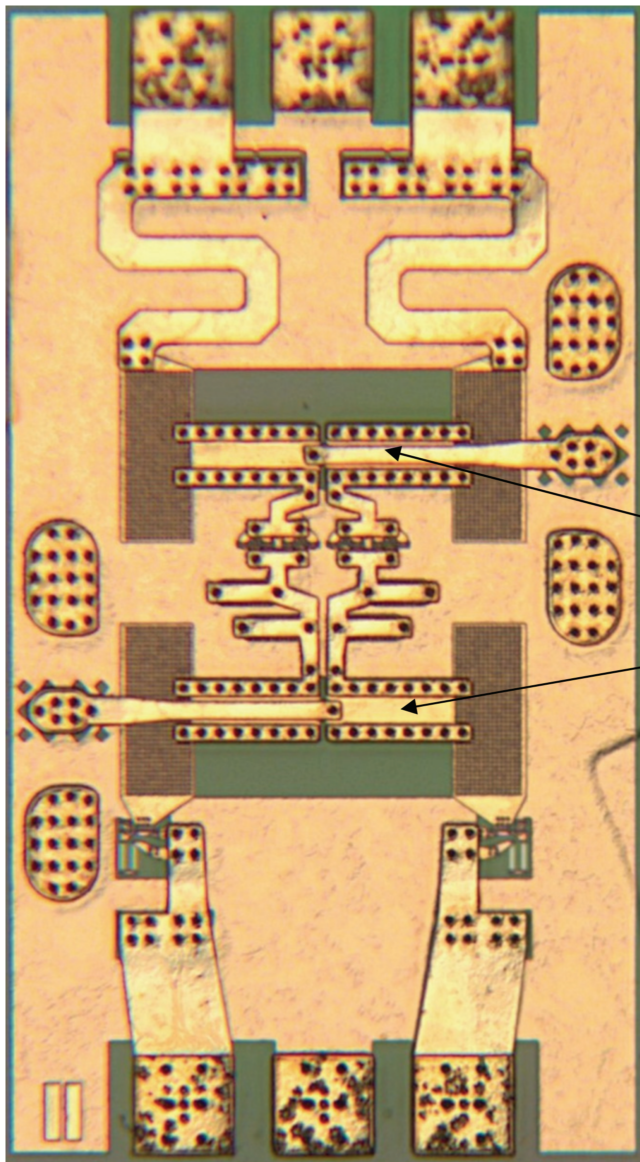
As with the transformer design,
each transistor is loaded in 25Ω
$\rightarrow$ 2:1 greater $N_E L_E$ than BJT that would drive 50Ω
$\rightarrow$ 2:1 greater P_{out} than BJT that would drive 50Ω

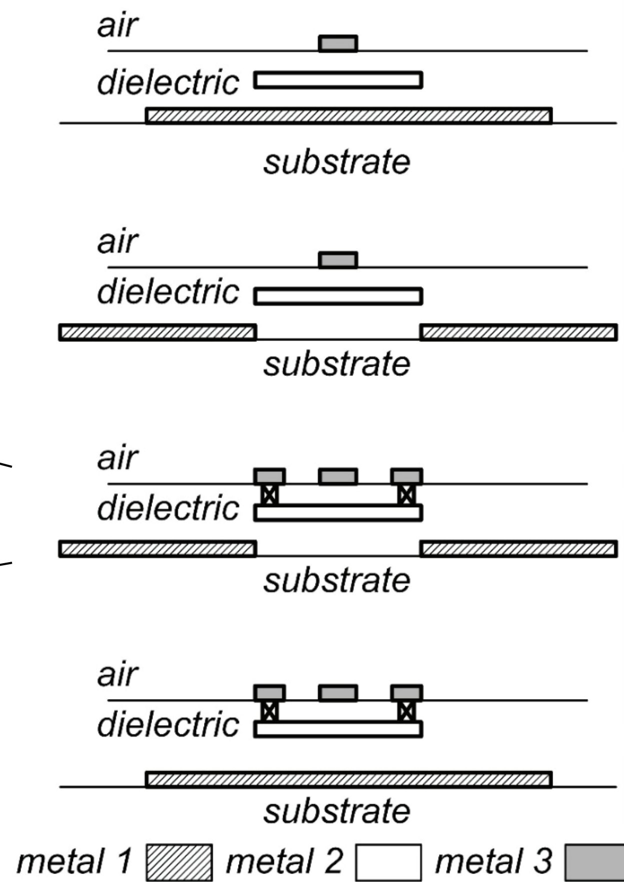
2 such BJTs.
$\rightarrow$ 4:1 greater P_{out} than BJT that would drive 50Ω

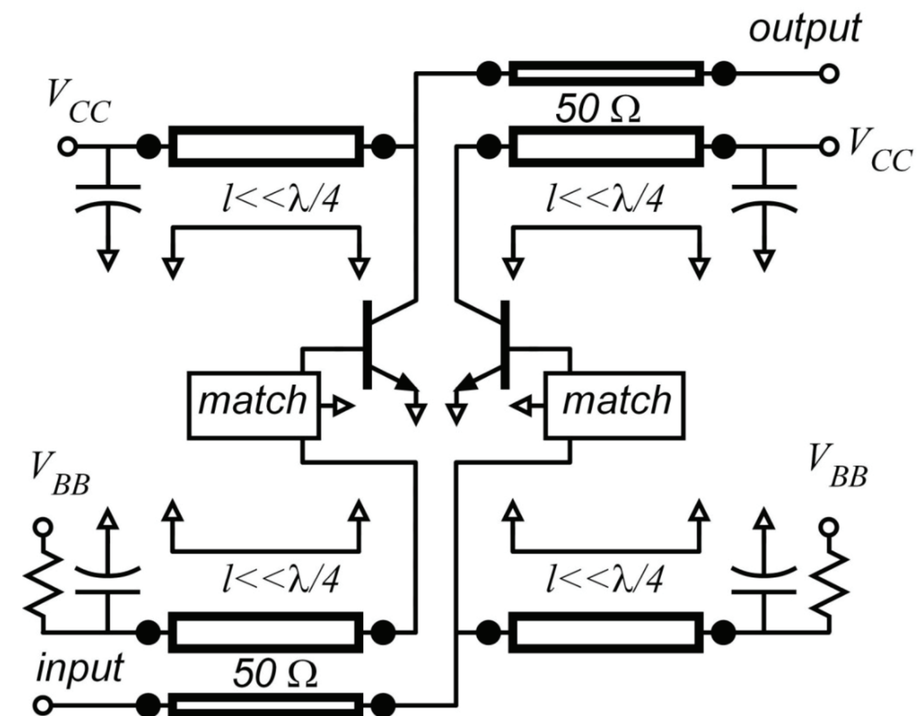
Note that baluns also provide DC bias feeds



Amplifier with 2:1 balun combiners







Park, IEEE JSSC 2018

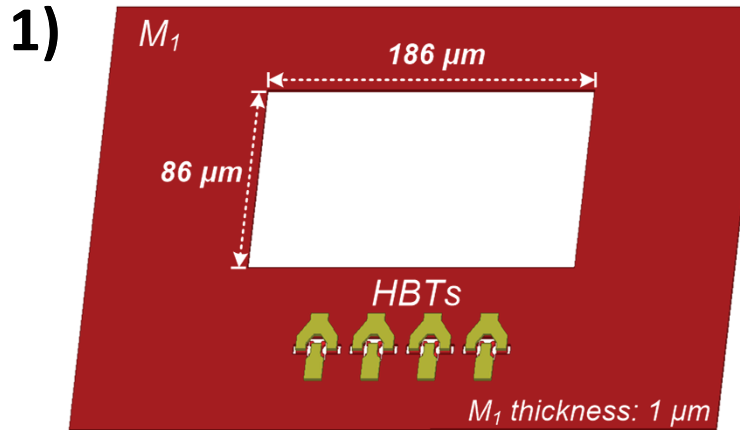
Amplifier with 2:1 balun combiners

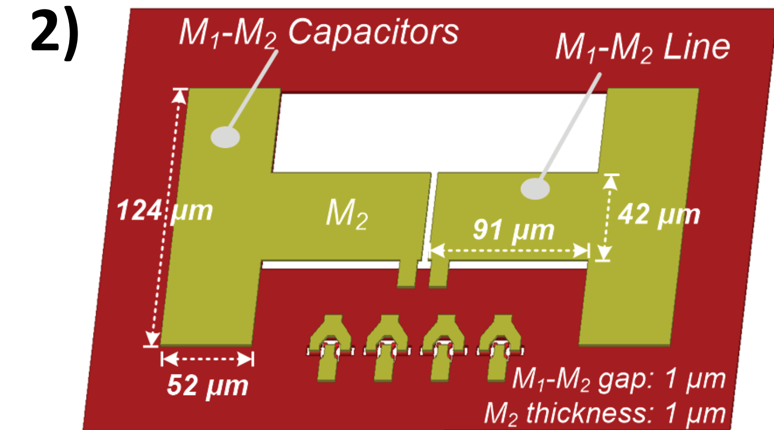
1) M_1 as a GND

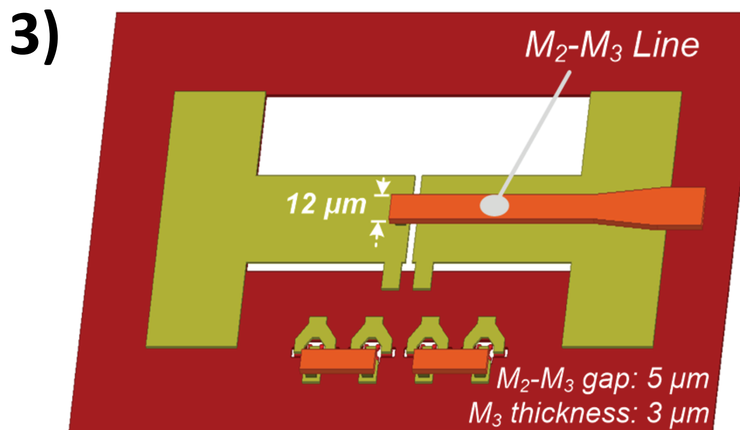
2) Slot-type transmission lines (M_1-M_2), AC shorts (2 pF MIM) at line ends.

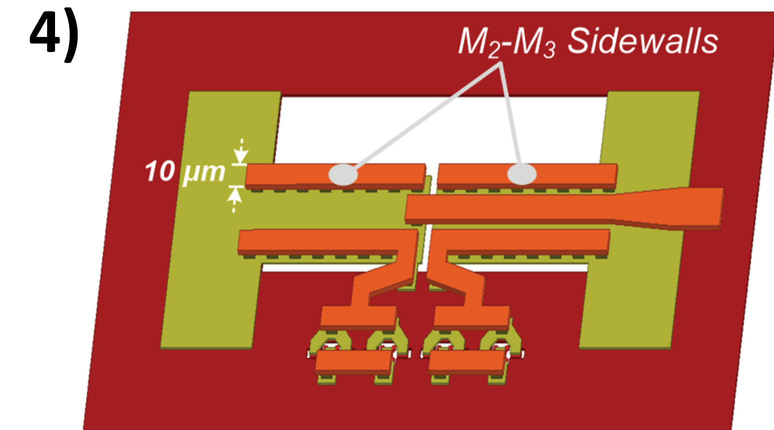
3) Microstrip line (M_2-M_3), E-field shielding

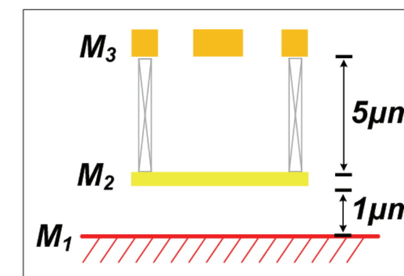
4) Side shields to prevent M_3-M_1 coupling





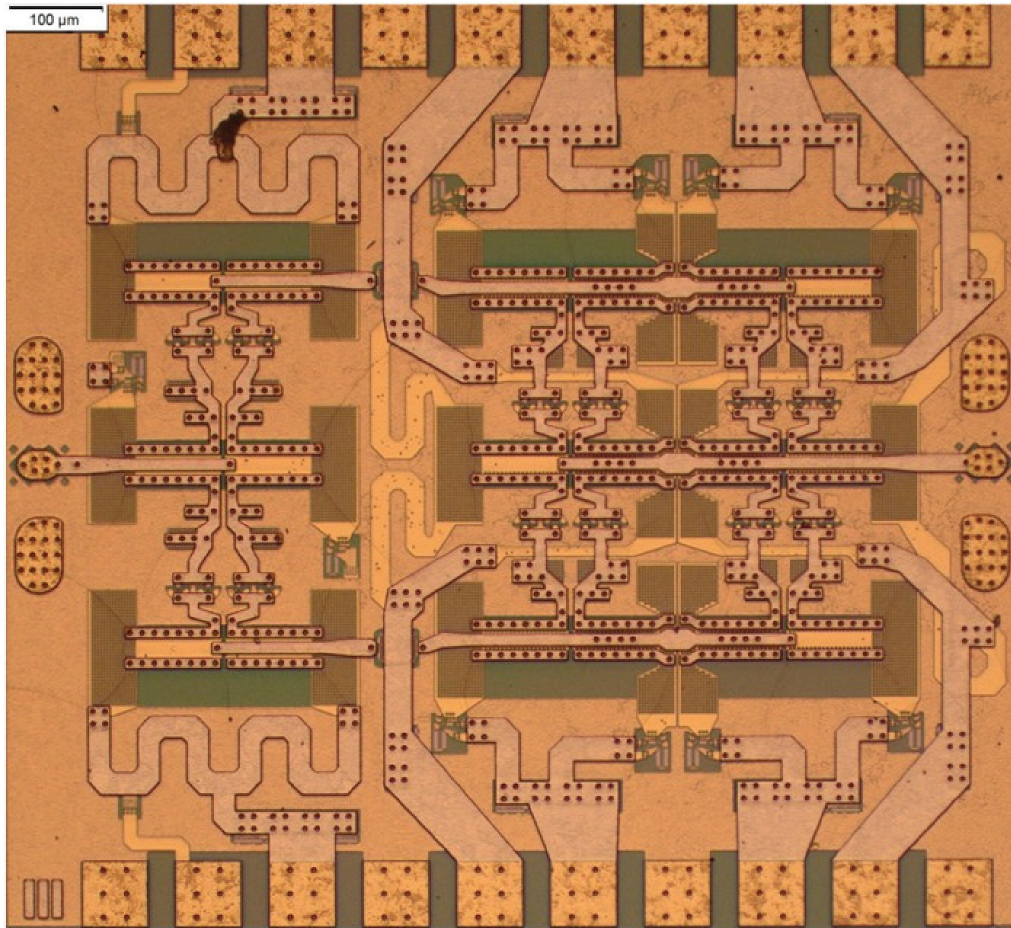


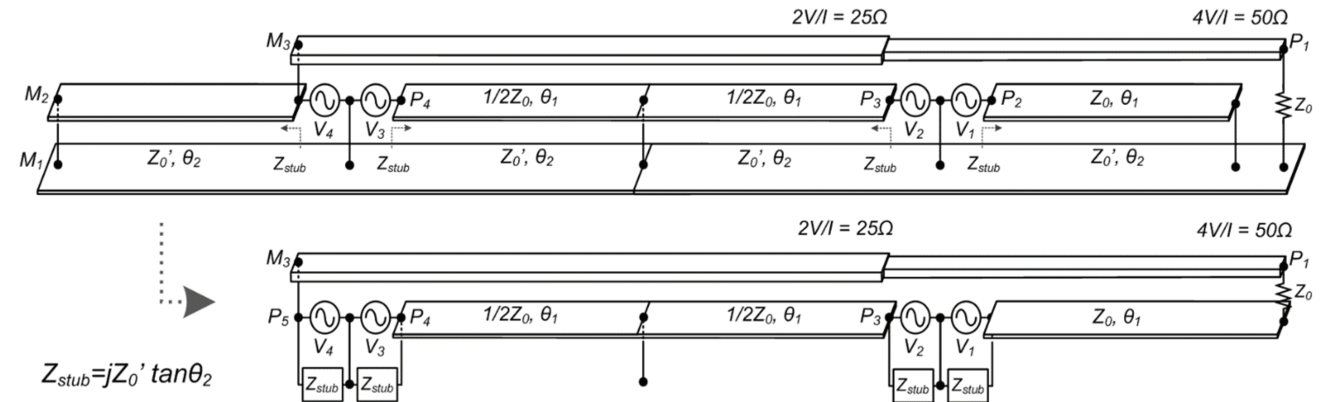


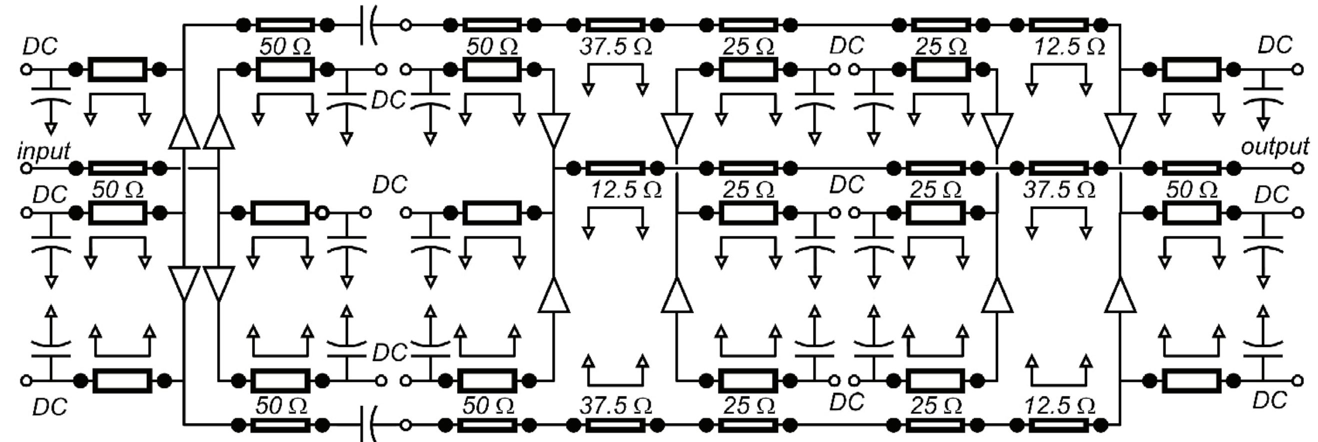


Park, IEEE JSSC 2018

Amplifier with balun combiners







Park, IEEE JSSC 2018

Linear and circular baluns

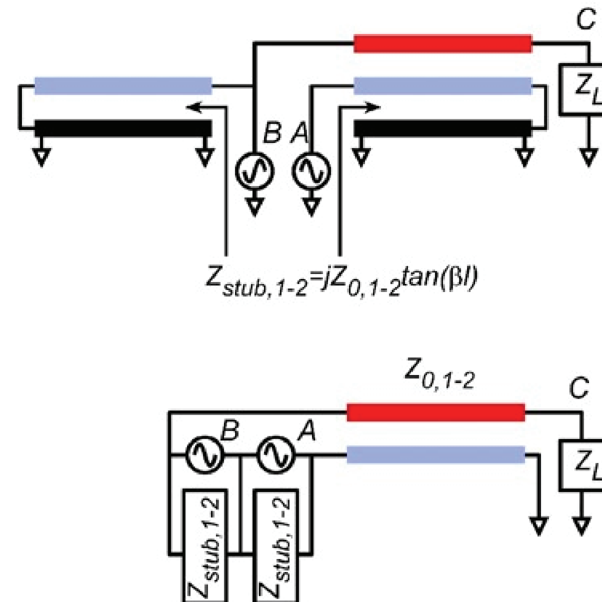
analysis: Park, IEEE JSSC 2018

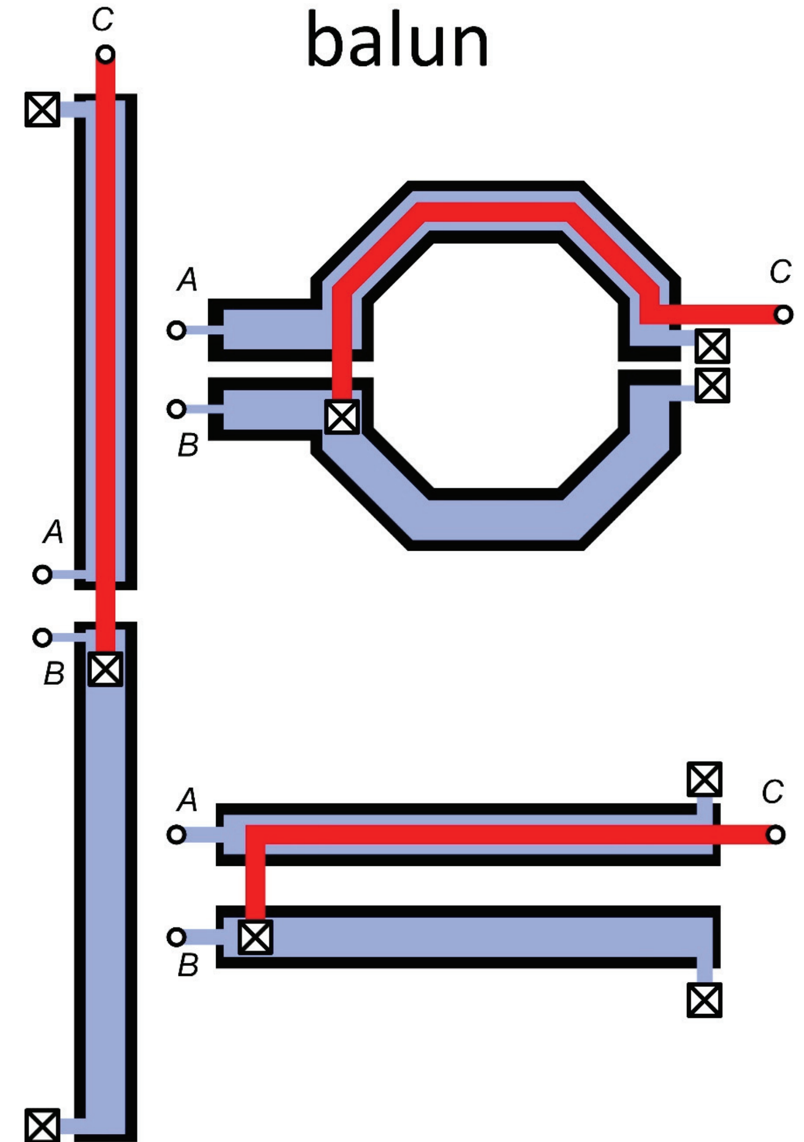
The two linear baluns are clearly electrically identical

...as is the round balun

The round balun seems to be similar
to a transformer.

This deserves further consideration





Circular balun

Daneshgar 2014 IEEE IMS symposium

This round balun seems to be very similar to a transformer....

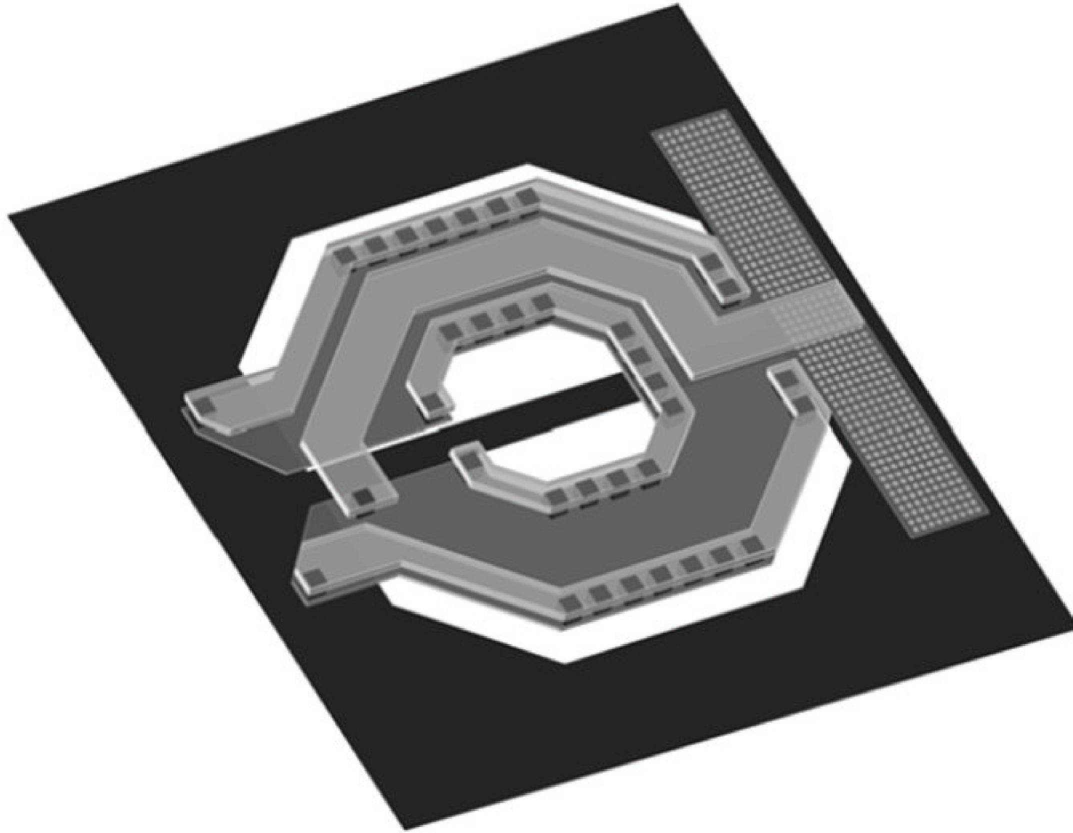
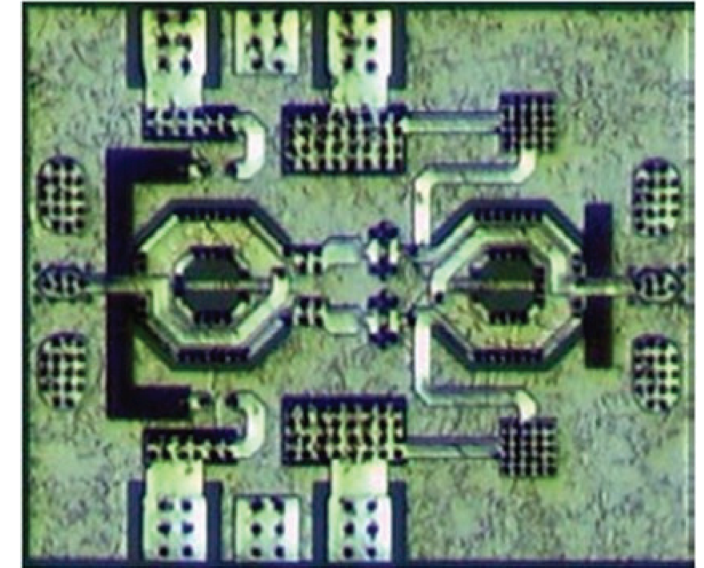


Fig. 2. Ring-shaped sub-λ/4 2-way balun.



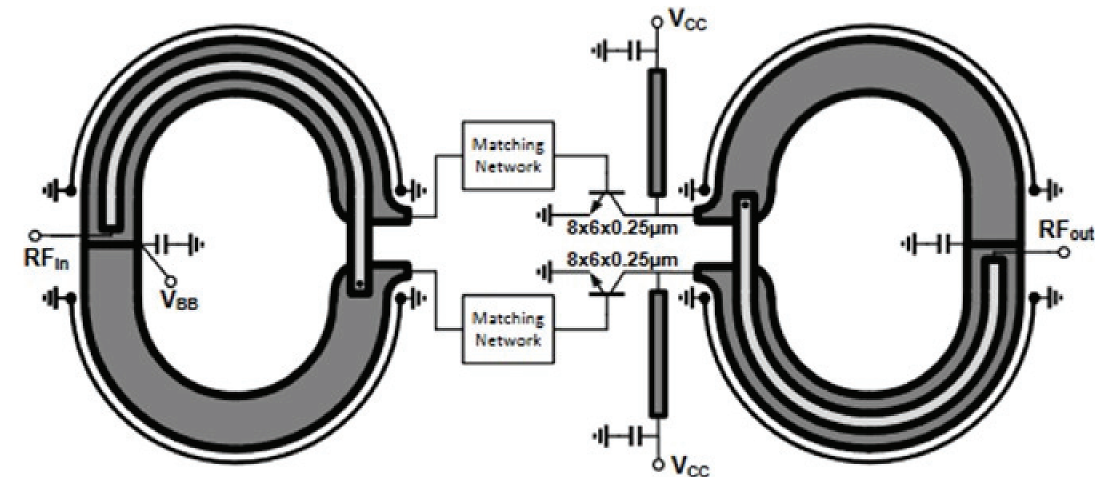


Fig. 3. Schematic diagram of the single-stage PA.

class notes, M. Rodwell, copyrighted 2012-2024

Transformers analyzed as multi-conductor lines (1)

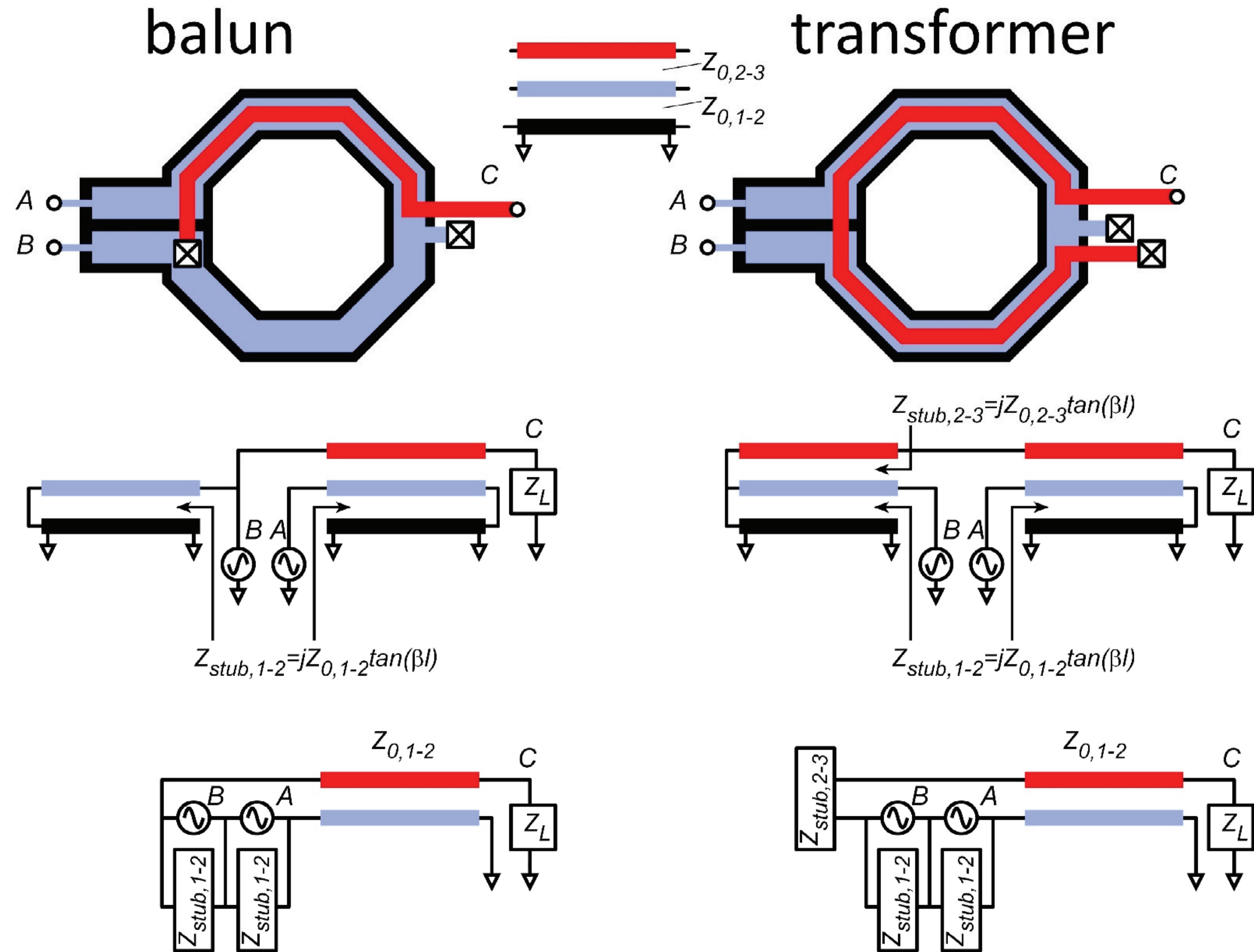
analysis: Park, IEEE JSSC 2018

Analyze both using modes on
3-conductor transmission-lines

Balun:
two shunt stubs

Transformer
two shunt stubs,
one series stub

Here, we have precisely defined
a constant m_1-to-m_2 separation distance,
i.e. the ground plane opening dimensions,
to precisely define $Z_{0,1-2}$



Transformers analyzed as multi-conductor lines (2)

analysis: Park, IEEE JSSC 2018

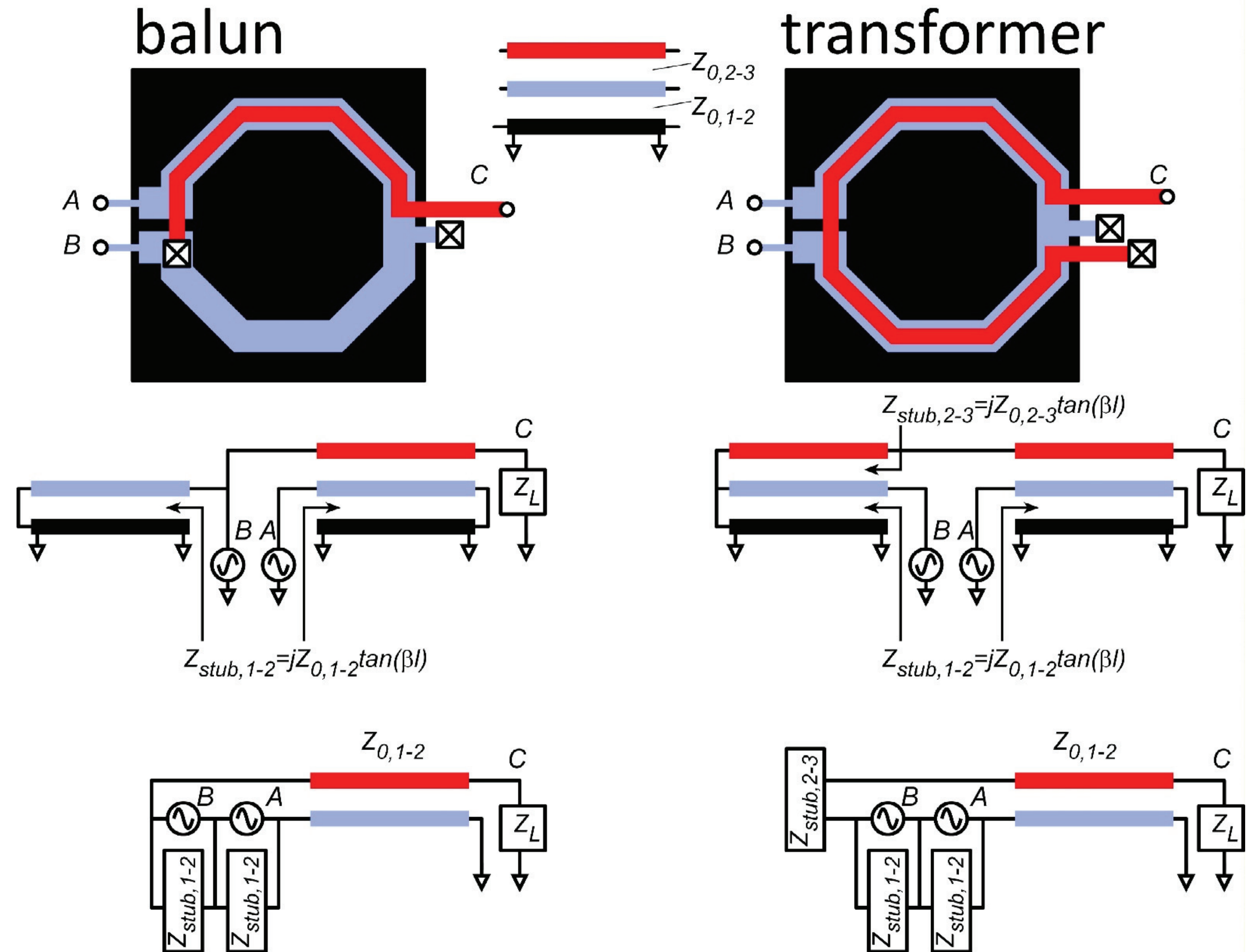
Analyze both using modes on
3-conductor transmission-lines

Balun:
two shunt stubs

Transformer
two shunt stubs,
one series stub

Here, as is more typical for transformers
we do not have constant m_1-to-m_2 separation,
so $Z_{0,1-2}$ is less to precisely defined.

This transformer equivalent circuit model
is nevertheless informative.

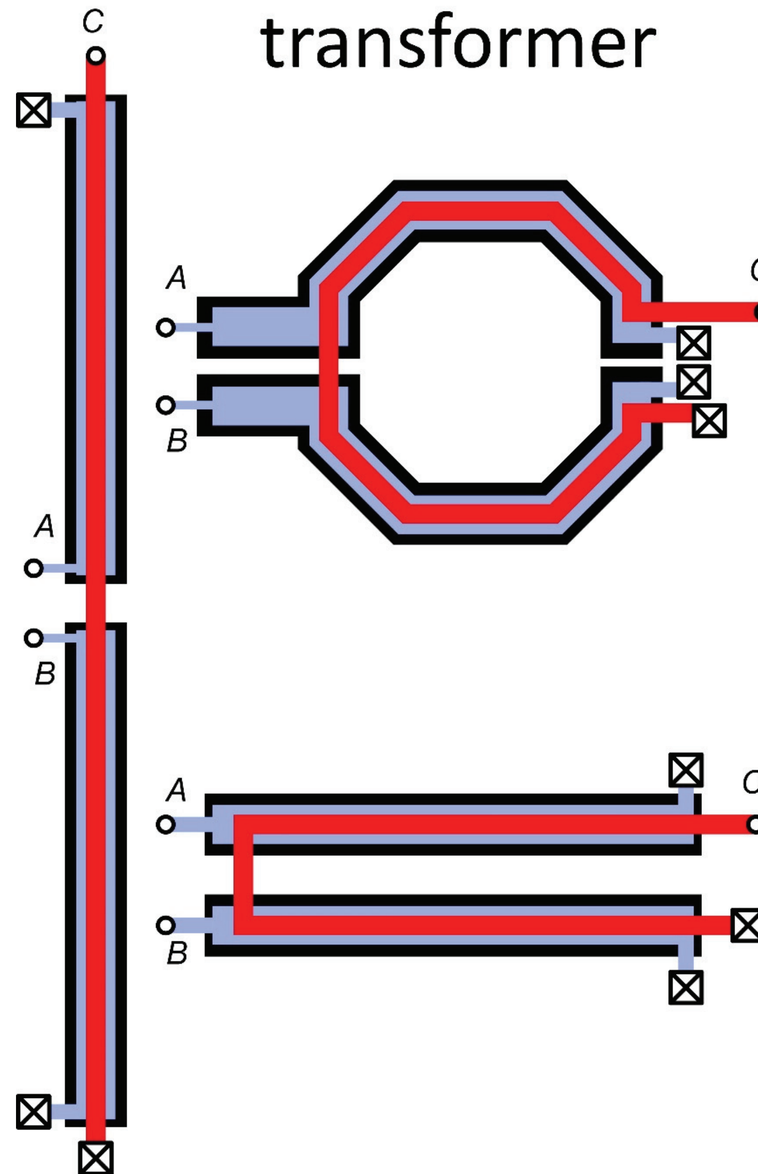


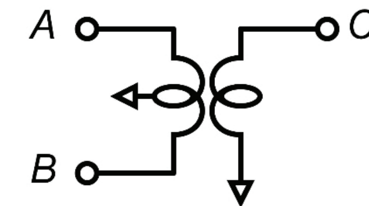
Transformers analyzed as multi-conductor lines (3)

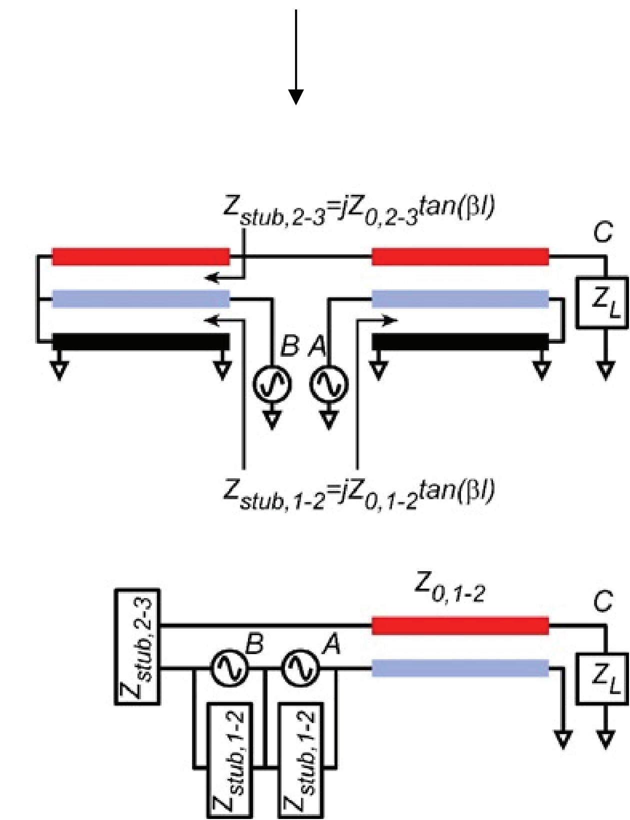
analysis: Park, IEEE JSSC 2018

Analyze transformer / balun using 3-conductor transmission-line models

Transformer:
two shunt stubs,
one series stub



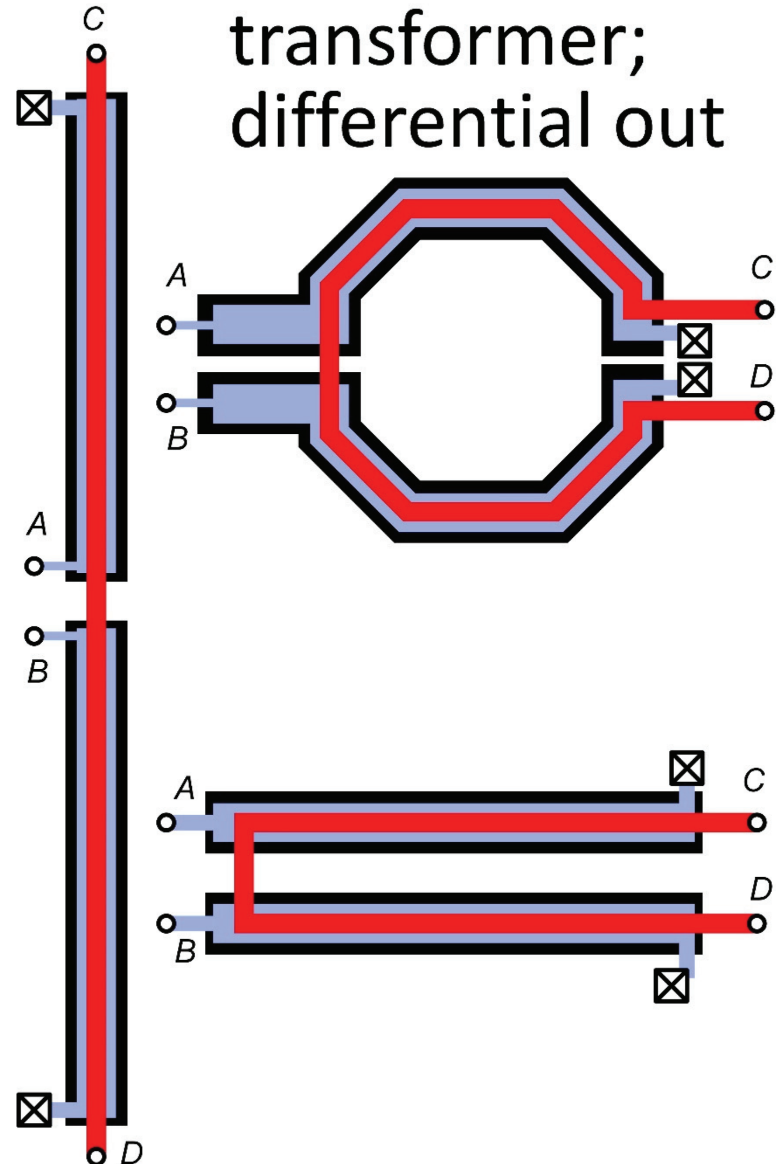


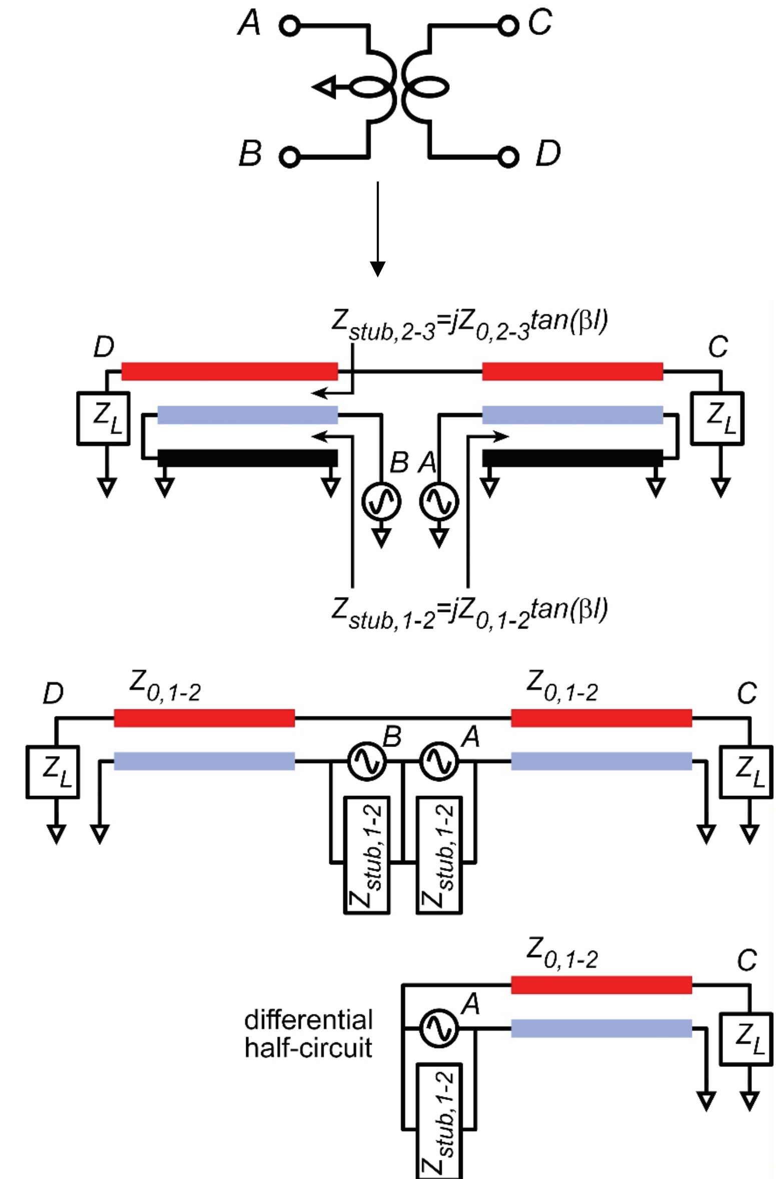


Differential Transformers as multi-conductor lines

analysis: Park, IEEE JSSC 2018

Transformer operation can be visualized, and analyzed, using multi-conductor line models



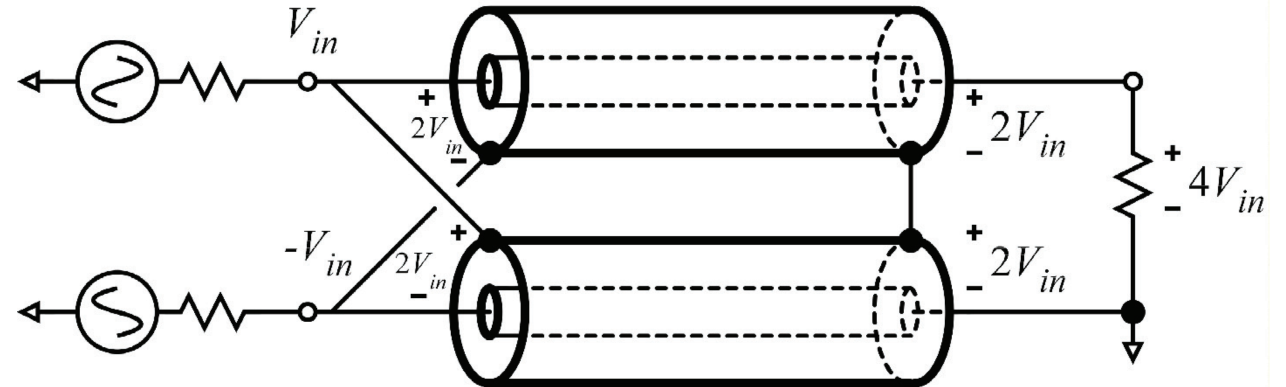


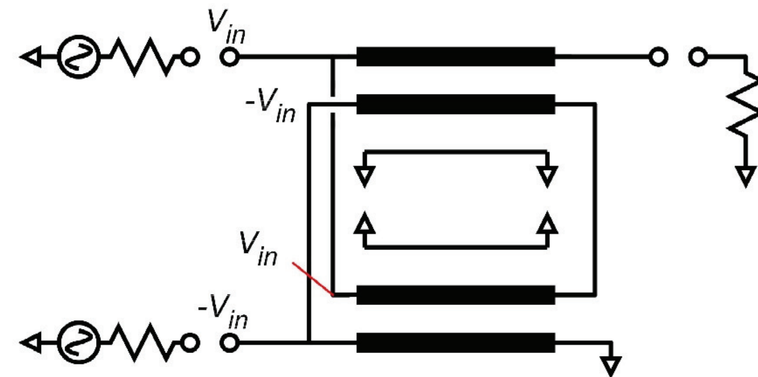
Other Transmission-line impedance transformers

Many such structures.

Widely used in 1970-1980's discrete-transistor RF PAs

See Motorola RF Device Data Handbook (1980's)





Other Transmission-line impedance transformers

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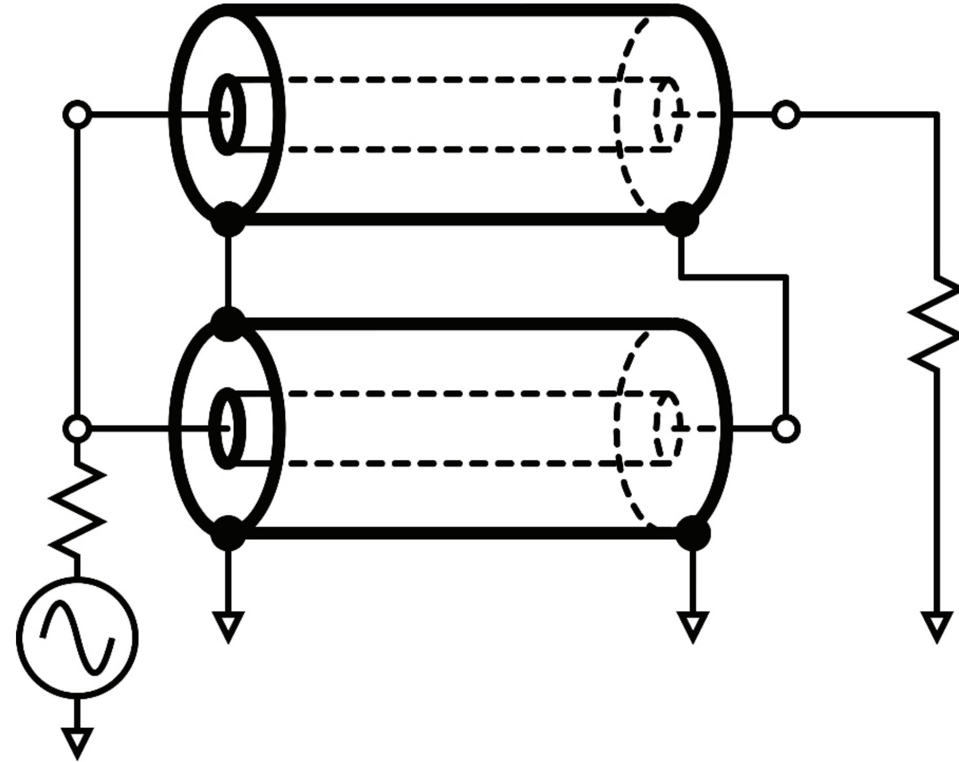


Transistor Series-Connections ("Stacking")

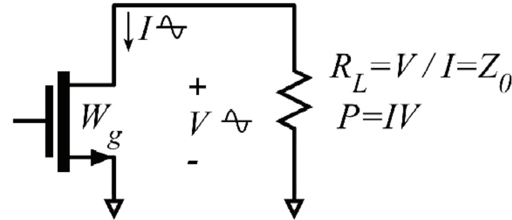
N parallel-connected transistors

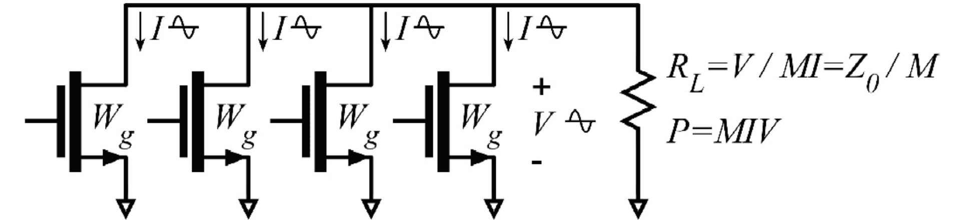
$$V_{out,pp} = (V_{\max} - V_{\min})$$

$$I_{out,pp} = NI_{\max}$$

$$P_{out} = V_{out,pp} I_{out,pp} / 8 = N(V_{\max} - V_{\min}) / I_{out,pp}$$

$$R_{load} = V_{out,pp} / I_{\max} = (V_{\max} - V_{\min}) / NI_{\max}$$





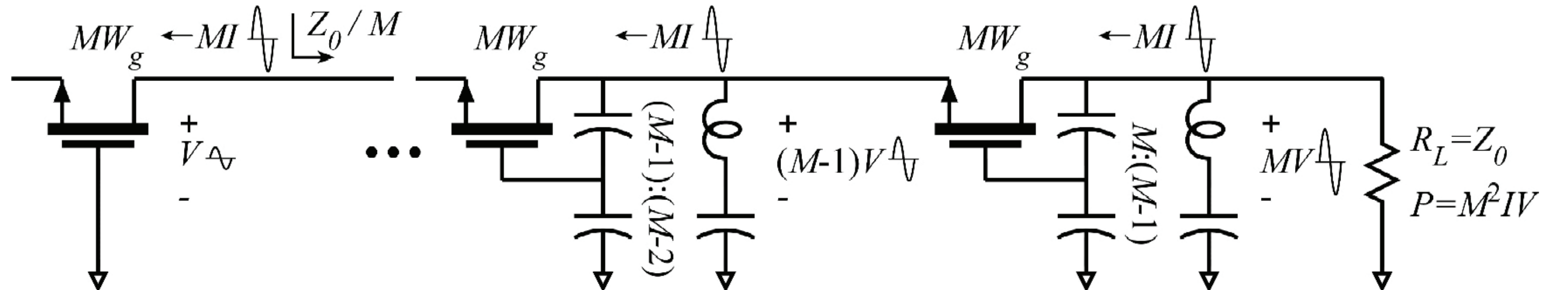
N series-connected transistors

$$V_{out,pp} = N(V_{\max} - V_{\min})$$

$$I_{out,pp} = I_{\max}$$

$$P_{out} = V_{out,pp} I_{out,pp} / 8 = N(V_{\max} - V_{\min}) / I_{out,pp}$$

$$R_{load} = V_{out,pp} / I_{\max} = N(V_{\max} - V_{\min}) / I_{\max}$$



High power obtained with higher external load impedances. Internal node impedances are lower

Capactive volage dividers provide appropriate voltage distribution. Inductors tune capacitors.

Design considerably more complex given transistor with parasitic R's and C's.

M. Shifrin et al, 1992 IEEE Microwave and Millimeter-Wave Monolithic Circuits Symp
S. Pornpromlikit et al, 2011 IEEE Compound Semiconductor Integrated Circuit Symp

Series amplifier design by 2-port techniques (1)

Ahmed S. H. Ahmed, 2018 EUMIC

First measure or simulate the transistor at desired output power.
Load pull simulation in common-base

Adjust Z_L for optimum P_{out} or optimum PAE.

Record *vector* (amplitude and phase)
values for $(V_{out,t}, V_{in,t}, I_{out,t}, I_{in,t})$

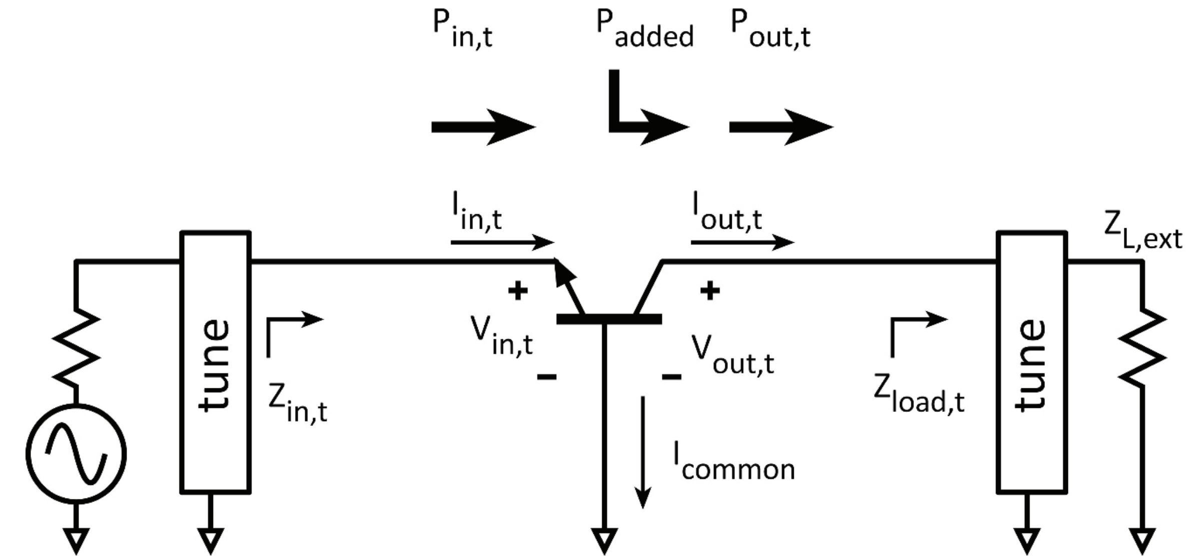
Equations use RMS quantities throughout $(V_{out,t}, V_{in,t}, I_{out,t}, I_{in,t})$
and, given large-signal operation, are vector amplitudes at f_{signal}

Define: $P_{in,t} = \mathrm{Re}\left(V_{in,t} I^*_{in,t}\right)$, $P_{out,t} = \mathrm{Re}\left(V_{out,t} I^*_{out,t}\right)$

Define: $P_{added} = P_{out,t} - P_{in,t}$

Optimum load impedance: $Z_{load,t} = V_{out,t} / I_{out,t}$

Transistor input impedance: $Z_{in,t} = V_{in,t} / I_{in,t}$

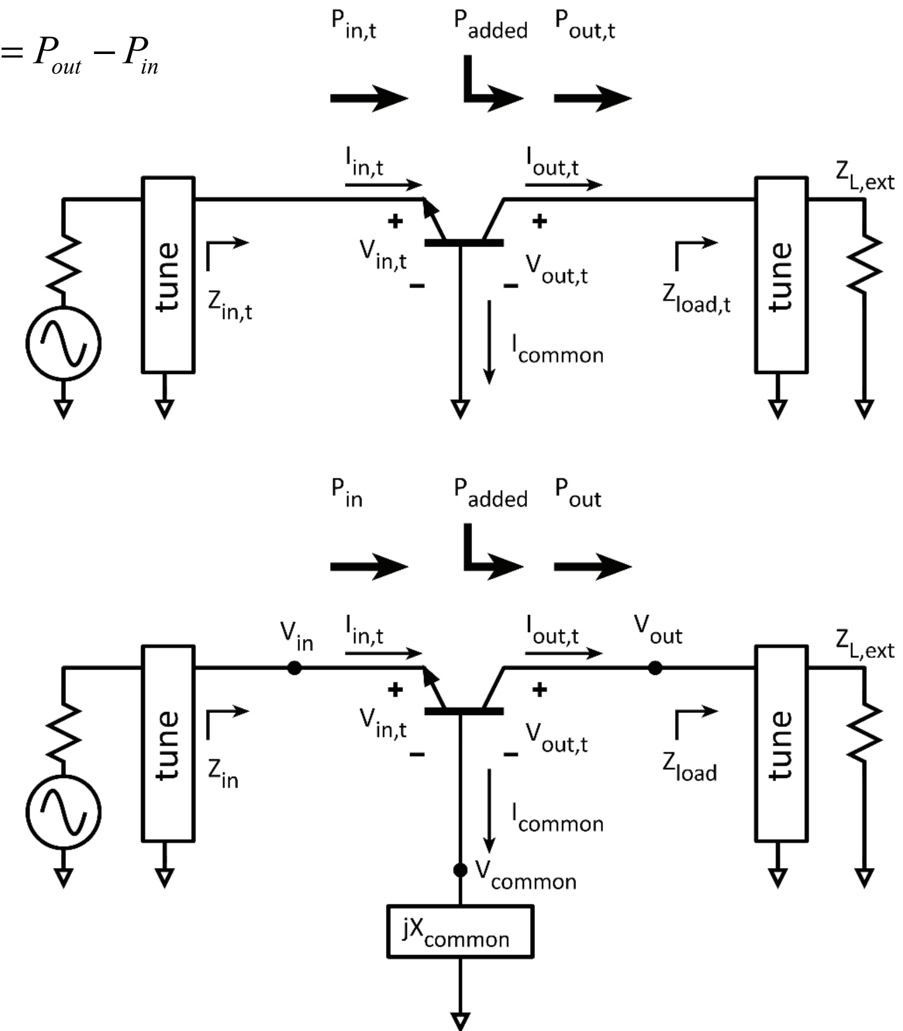


Series amplifier design by 2-port techniques (2)

Ahmed S. H. Ahmed, 2018 EUMIC

For some stage, select some $P_{out} > P_{out,t}$,

we then have: $V_{in} = V_{in,t} + V_{common}$, $V_{out} = V_{out,t} + V_{common}$, $P_{in} = \mathrm{Re}(V_{in} I^*_{in,t})$, $P_{out} = \mathrm{Re}(V_{out} I^*_{out,t})$, $P_{added} = P_{out} - P_{in}$



Required common-lead impedance jX_{common}

$$P_{out} = \mathrm{Re}(V_{out} I^*_{out,t}) = \mathrm{Re}(V_{out,t} I^*_{out,t} + V_{common} I^*_{out,t}) = \mathrm{Re}(V_{out,t} I^*_{out,t} + jX_{common} I_{common} I^*_{out,t})$$

$$P_{out} = \mathrm{Re}(V_{out,t} I^*_{out,t} - V_{in,t} I^*_{in,t} + jX_{common} I_{common} I^*_{out,t} + V_{in,t} I^*_{in,t}) = \mathrm{Re}(P_{added} + V_{in,t} I^*_{in,t} + jX_{common} I_{common} I^*_{out,t})$$

$$P_{out} - P_{out,t} = \mathrm{Re}(jX_{common}(I_{out,t} - I_{in,t}) I^*_{out,t}) = \mathrm{Re}(jX_{common}(I_{out,t} I^*_{out,t} - I_{in,t} I^*_{out,t}))$$

$$X_{common} = \frac{P_{out} - P_{out,t}}{\mathrm{Re}(j(I_{out,t} I^*_{out,t} - I_{in,t} I^*_{out,t}))} = \frac{P_{out} - P_{out,t}}{\mathrm{Im}(I_{out,t} I^*_{out,t} - I_{in,t} I^*_{out,t})}$$

Required transistor load impedance:

$$Z_{Load} = V_{out} / I_{out,t} = V_{out,t} / I_{out,t} + V_{common} / I_{out,t} = V_{out,t} / I_{out,t} + jX_{common} I_{common} / I_{out,t}$$

$$= V_{out,t} / I_{out,t} + jX_{common}(I_{in,t} - I_{out,t}) / I_{out,t} = V_{out,t} / I_{out,t} + jX_{common}(I_{in,t} / I_{out,t} - 1)$$

$$= Z_{Load,t} + jX_{common}(I_{in,t} / I_{out,t} - 1)$$

Resulting input impedance:

$$Z_{in} = V_{in} / I_{in,t} = V_{in,t} / I_{in,t} + V_{common} / I_{in,t} = V_{in,t} / I_{in,t} + jX_{common} I_{common} / I_{in,t}$$

$$= V_{in,t} / I_{in,t} + jX_{common}(I_{in,t} - I_{out,t}) / I_{in,t} = V_{in,t} / I_{in,t} + jX_{common}(1 - I_{out,t} / I_{in,t})$$

$$= Z_{in,t} + jX_{common}(1 - I_{out,t} / I_{in,t})$$

Series amplifier design by 2-port techniques (3)

Ahmed S. H. Ahmed, 2018 EUMIC

Stack synthesis: # emitter fingers: $N_E, N_{E1}, N_{E2}, N_{E3}$. Emitter length per finger: $L_E, L_{E1}, L_{E2}, L_{E3}$

As long as DC currents are isolated between stages, $N_E L_E$ can differ between stages

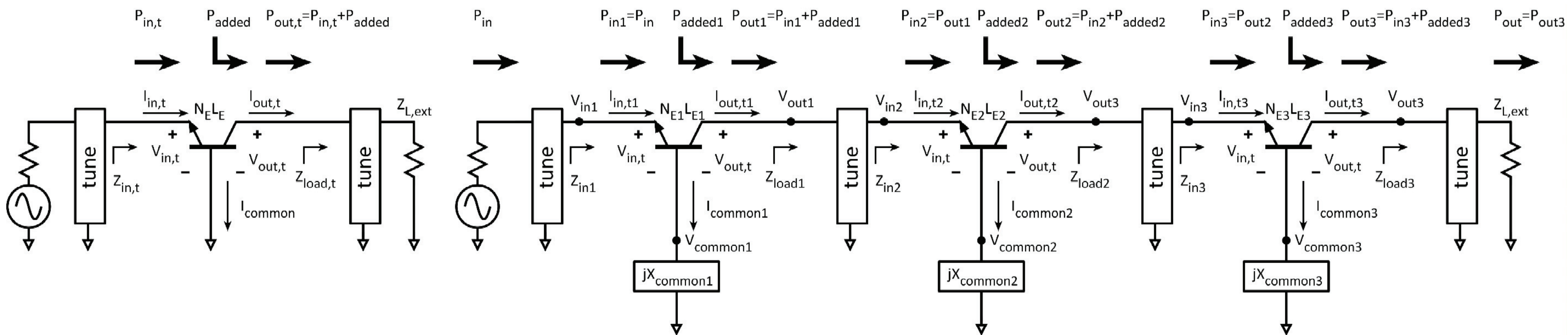
This gives:

$$I_{out3} / N_{E3}L_{E3} = I_{out2} / N_{E2}L_{E2} = I_{out1} / N_{E1}L_{E1} = I_{out} / N_E L_E$$

$$I_{in3} / N_{E3}L_{E3} = I_{in2} / N_{E2}L_{E2} = I_{in1} / N_{E1}L_{E1} = I_{in} / N_E L_E$$

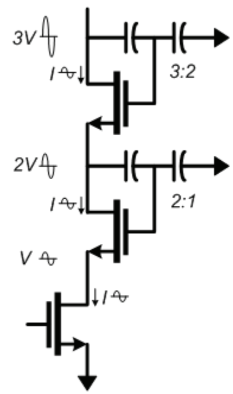
$$P_{Added3} / N_{E3}L_{E3} = P_{Added2} / N_{E2}L_{E2} = P_{Added1} / N_{E1}L_{E1} = P_{Added} / N_E L_E$$

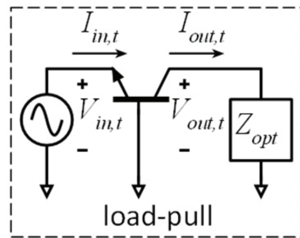
Stages can be designed to add power in any desired progression $P_{in}, P_{out1}, P_{out2}, P_{out3}$, ... as long as $P_{outN} / P_{out,(N-1)} \leq P_{out,T} / P_{in,T}$

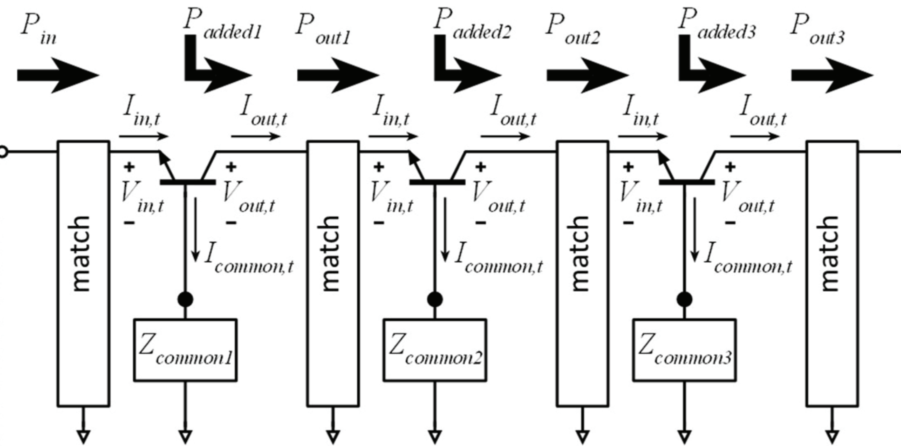


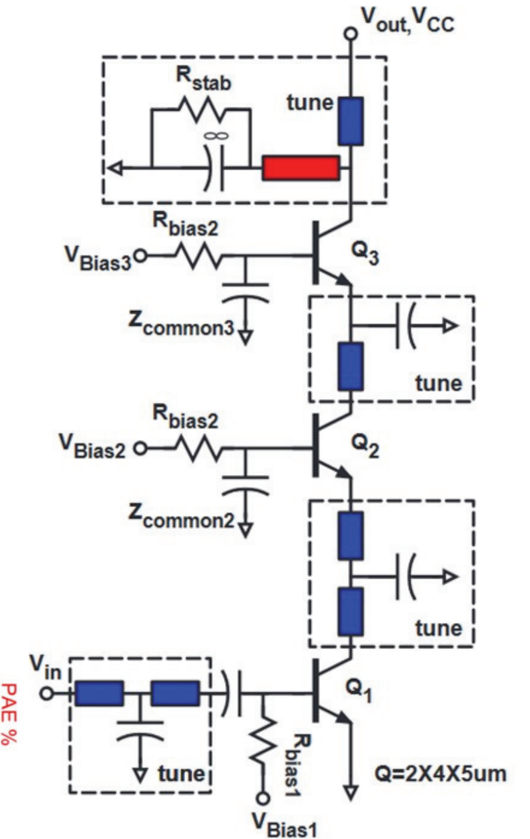
Cascade combining as stacking plus matching

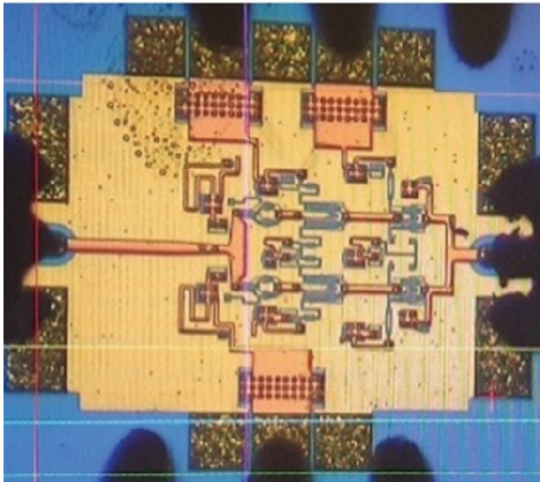
A. S. H. Ahmed et al., 2018 EuMIC (UCSB)

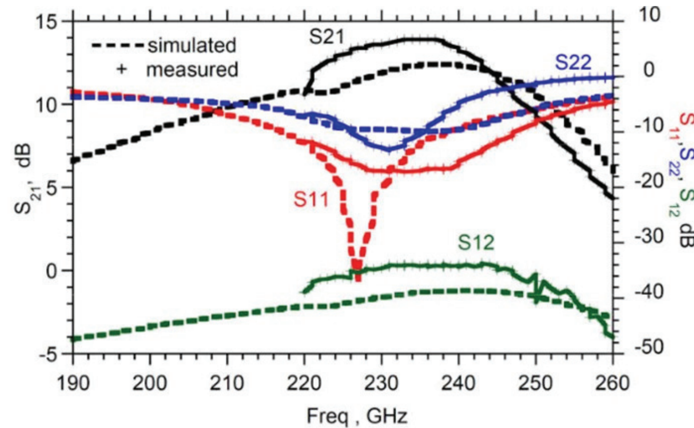


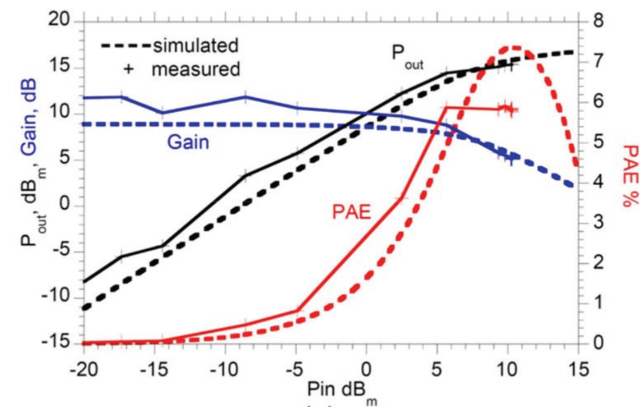








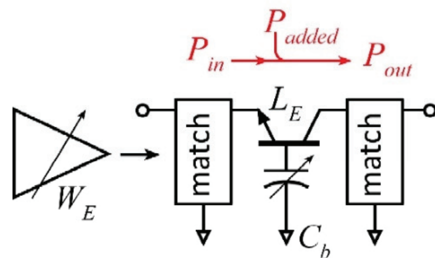




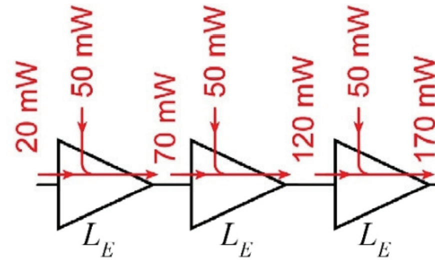
Generalized cascade combining

A. S. H. Ahmed et al, 2018 EuMIC (UCSB)
A. S. H. Ahmed, et al, 2021 RFIC Symposium

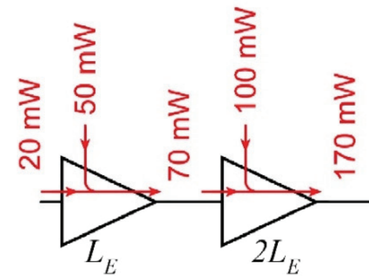
adjustable power summation



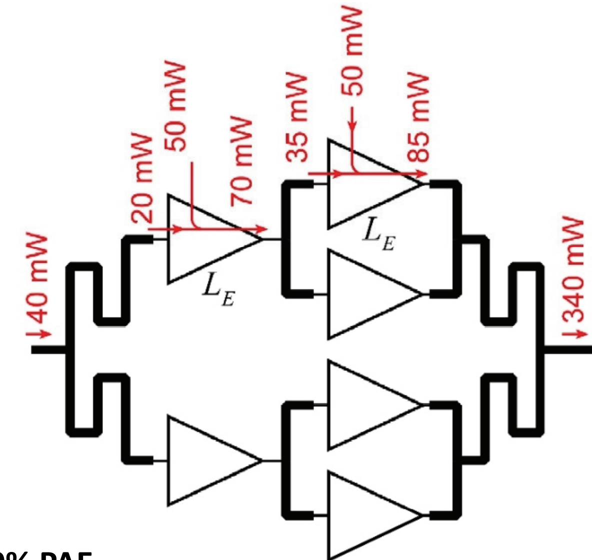
=stacking + matching

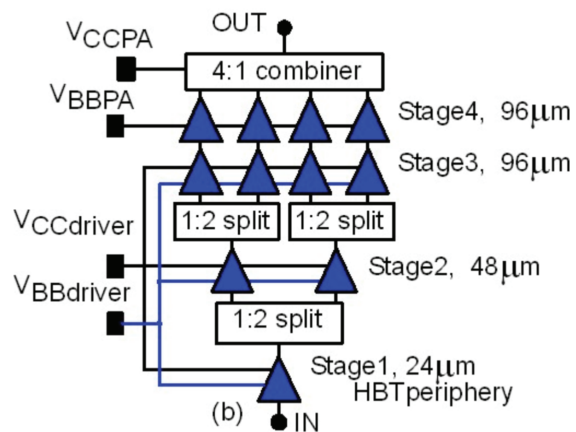


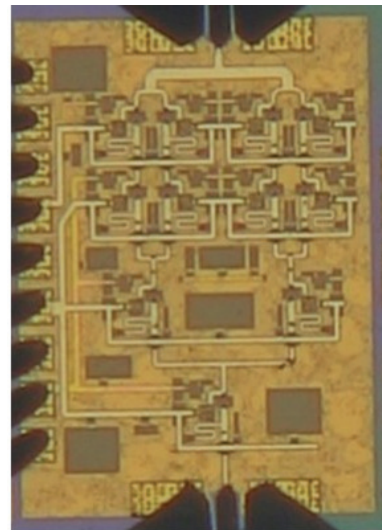
nonuniform



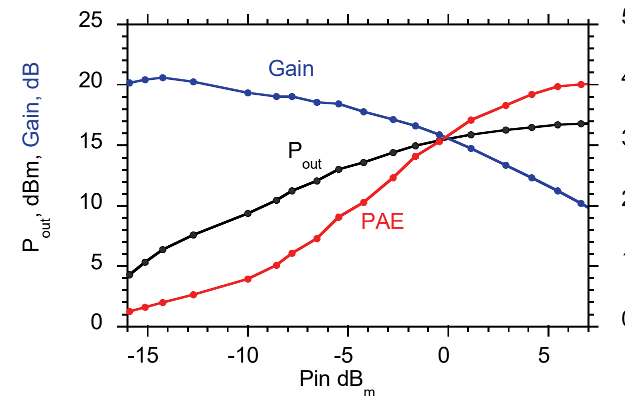
with spittling or combining

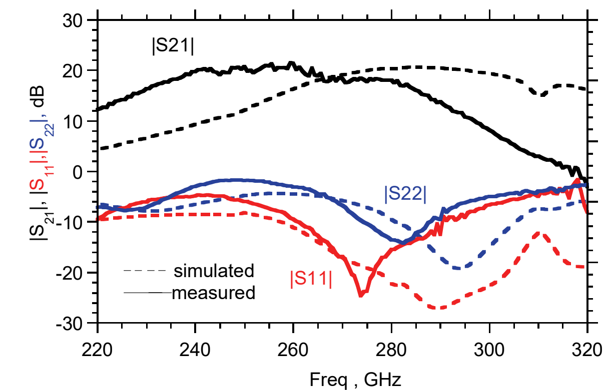






266GHz, 16.8dBm, 4.0% PAE

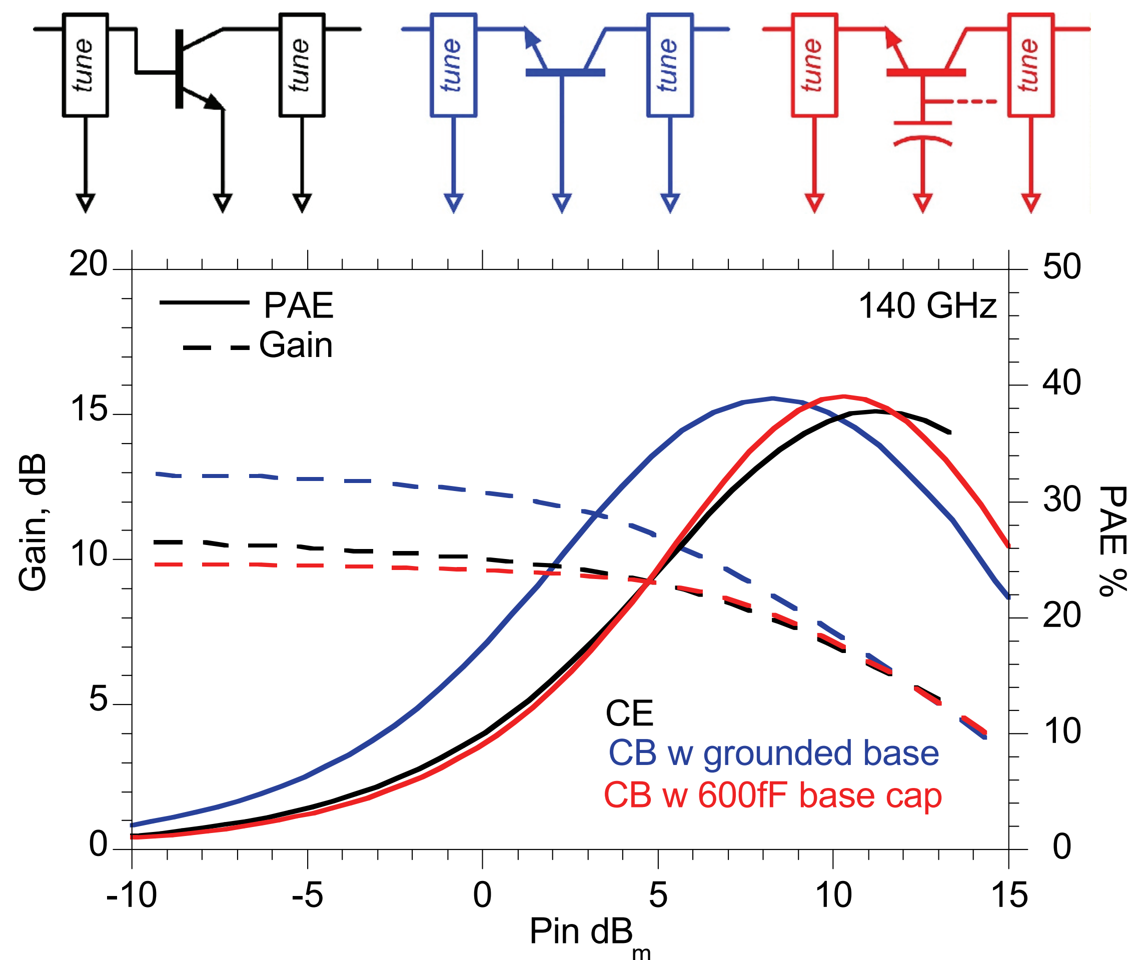


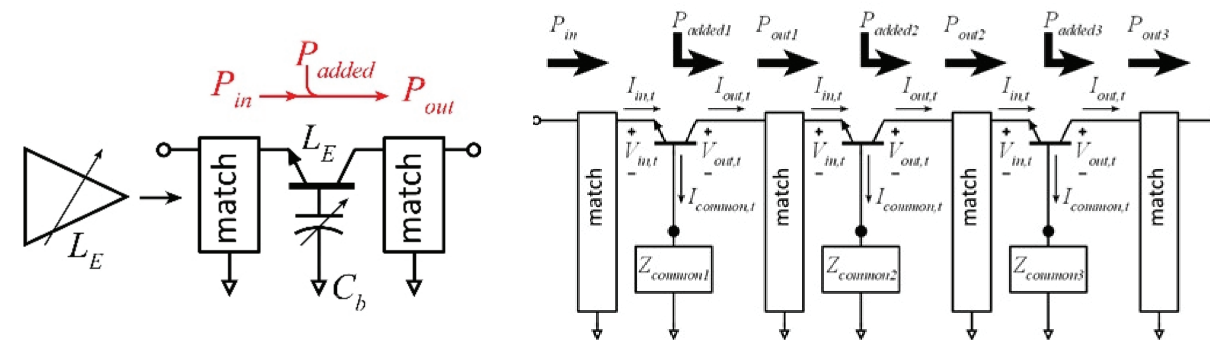


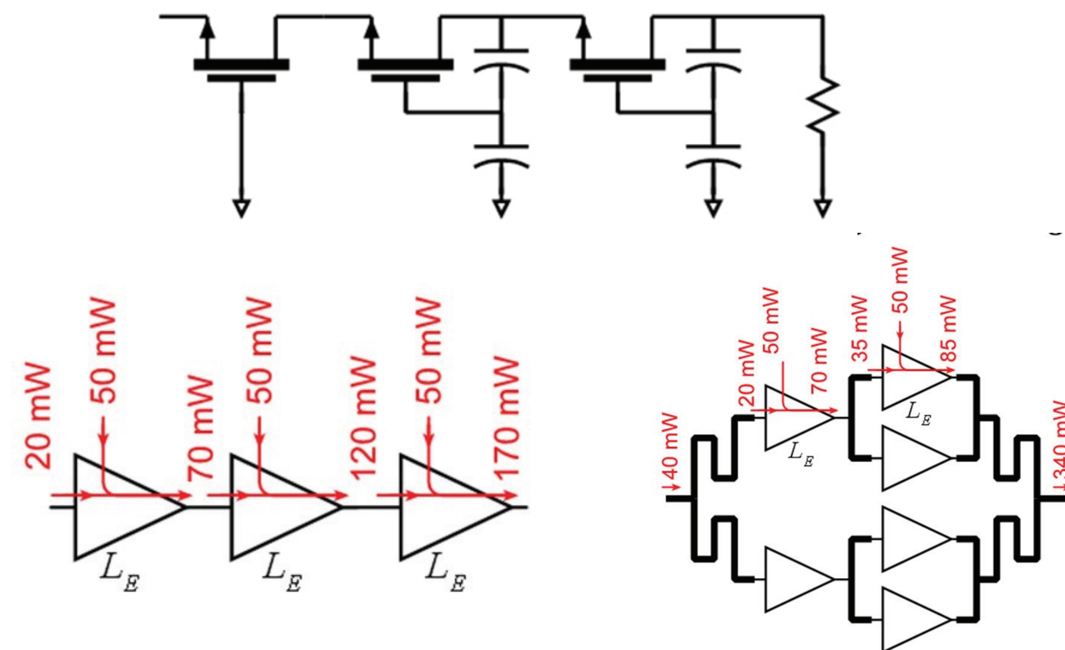
Capacitively degenerated common-base = cascade combining

Lower gain, same peak PAE, higher PAE at P_{1dB}.

This is the same as cascade combining.







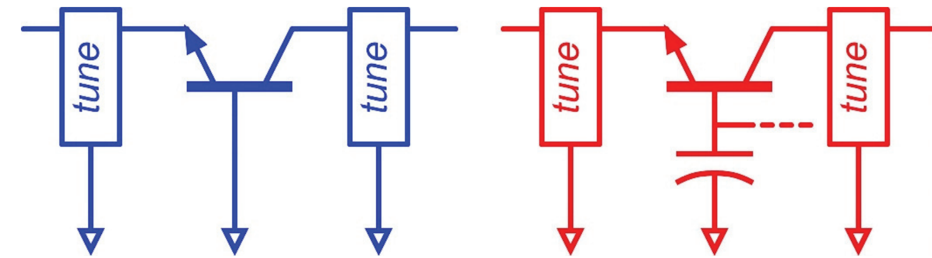
Capacitive degeneration: optimum gain

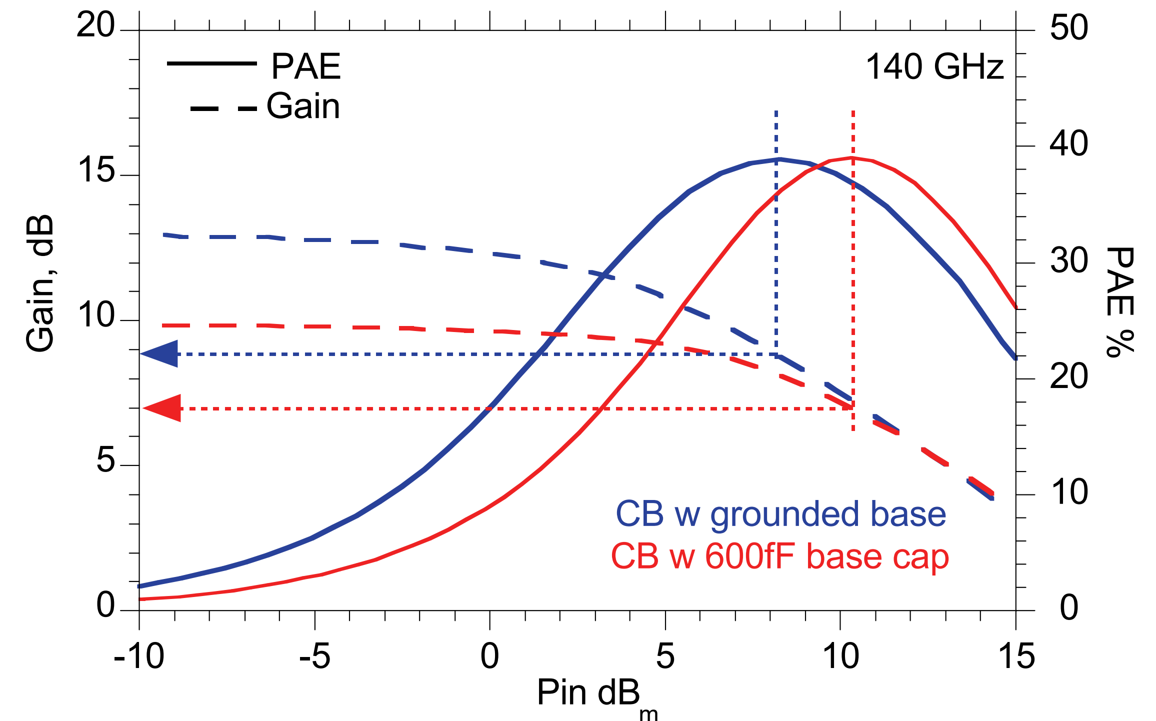
Capacitive degeneration:
no effect on peak PAE....given lossless embedding

No capacitive degeneration:
more gain compression @ P_{1dB}. ✗
more gain @ P_{1dB} ✓
input matching losses have less effect on PAE ✓

With capacitive degeneration:
less gain compression @ P_{1dB}. ✓
less gain @ P_{1dB} ✗
input matching losses have more effect on PAE ✗

Design for greatest PAE @ P_{1dB}
balances these two considerations.





Other cascade combining forms: useful & not.

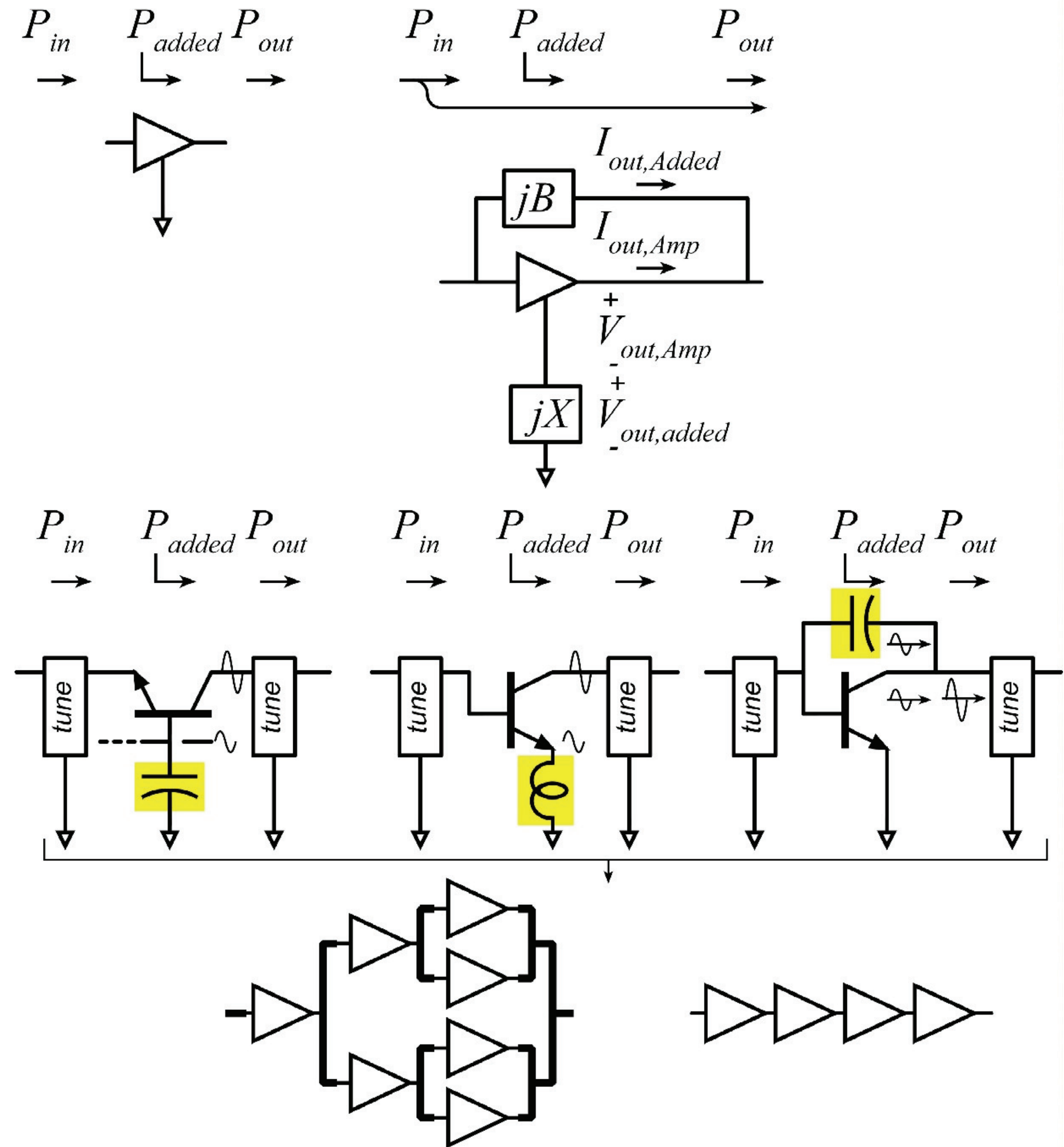
Series reactance: voltages add, Z_{load} increases.
output powers add if $V_{\text{out,Amp}}$ & V_{added} are in phase.

Shunt reactance: currents add, Z_{load} decreases.
output powers add if $I_{\text{out,Amp}}$ & I_{added} are in phase.

Even simple C_{cb}/C_{gd} feed-forward sums powers…
….if $I_{\text{out,Amp}}$ & I_{added} are not exactly in quadrature

$$\text{PAE} = \eta_{\text{collector/drain}} \cdot \left(1 - \frac{1}{G}\right)$$

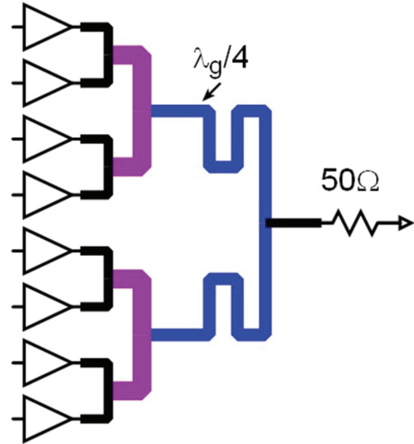
Lossless embedding: PAE is fixed, but G and η vary.
→ η is not a useful measure of transistor peformance



class notes, M. Rodwell, copyrighted 2012-2024

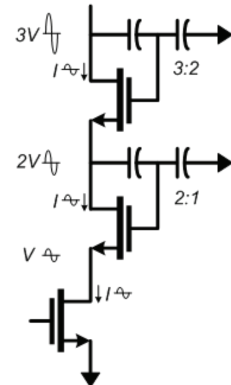
Power combining methods

Corporate T-line



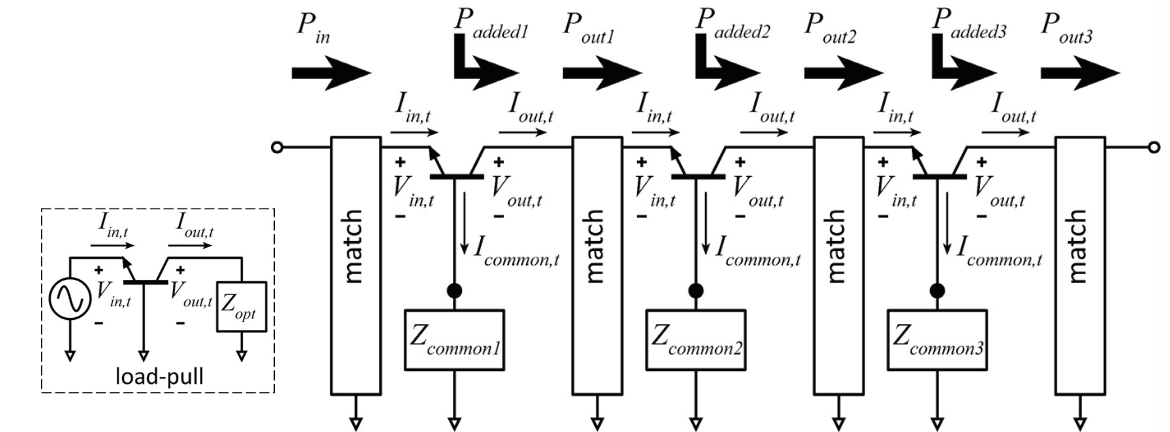
Direct series-connected

M. Shifrin: 1992 IEEE μWave/mmWave Monolithic Circuits Symp.



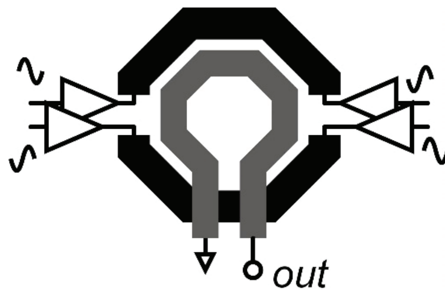
Cascaded combining

A. Ahmed 2018 EuMIC, 2021 RFIC



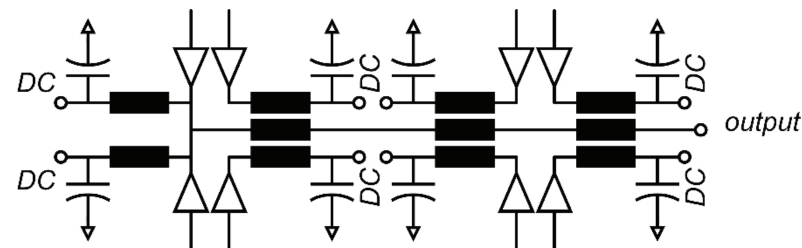
Distributed Active Transformer

I. Aoki, IEEE Trans MTT, Jan. 2002



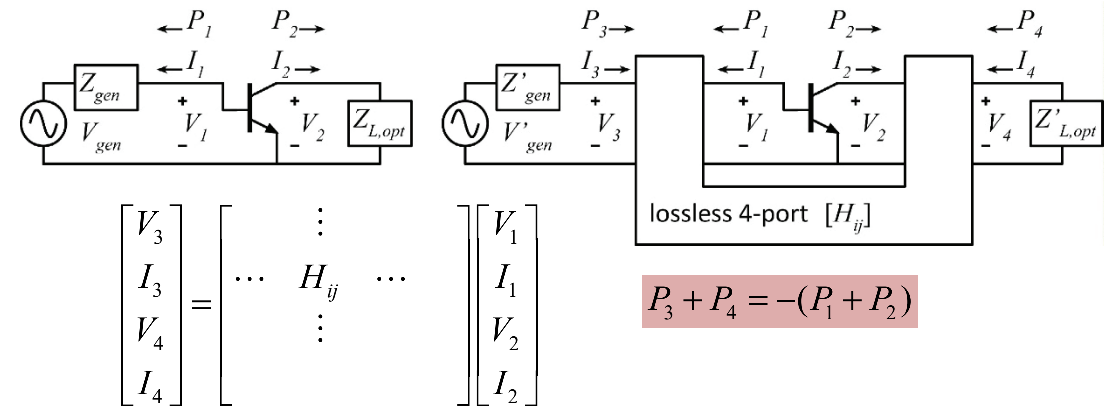
Balun series-connected

λ/4 baluns: Y. Yoshihara, 2008 IEEE Asian Solid-State Circuits Conference
sub-λ/4 baluns: H. Park, et al., IEEE JSSC, Oct. 2014



Invariance of PAE vs. added power

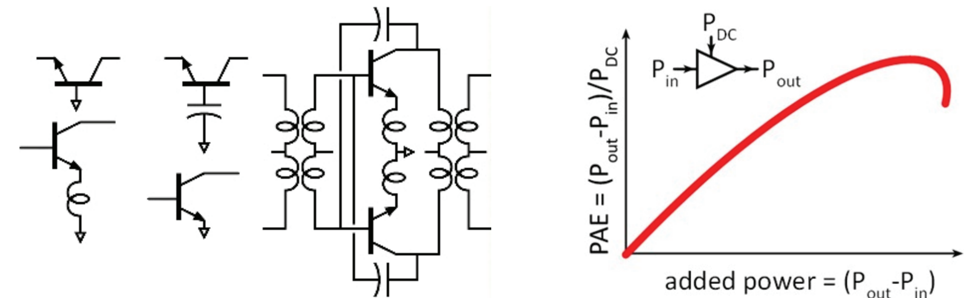
Given the correct source and load impedances,
all (lossless) power amplifier circuits have the same maximum efficiency vs. added power curve.



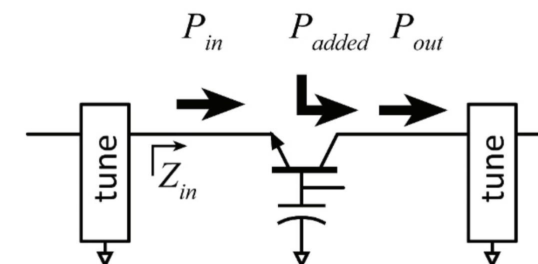
$$\begin{bmatrix} V_3 \\ I_3 \\ V_4 \\ I_4 \end{bmatrix} = \begin{bmatrix} & \vdots & \\ \cdots & H_{ij} & \cdots \\ & \vdots & \end{bmatrix} \begin{bmatrix} V_1 \\ I_1 \\ V_2 \\ I_2 \end{bmatrix}$$

$$(V_1, V_2, I_1, I_2, H_{ij}) \rightarrow (V_3, V_4, I_3, I_4, Z'_{L,opt}, P_{in}, Z_{in})$$

Things that don't change PAE:
Source/emitter inductance in common-source/emitter
Base/gate capacitance in common base/gate.
Capacitive neutralization
Singhakowinta's unconditionally stable positive feedback.



Design goal:
amplifier PAE close to transistor PAE
minimize tuning and power combining losses



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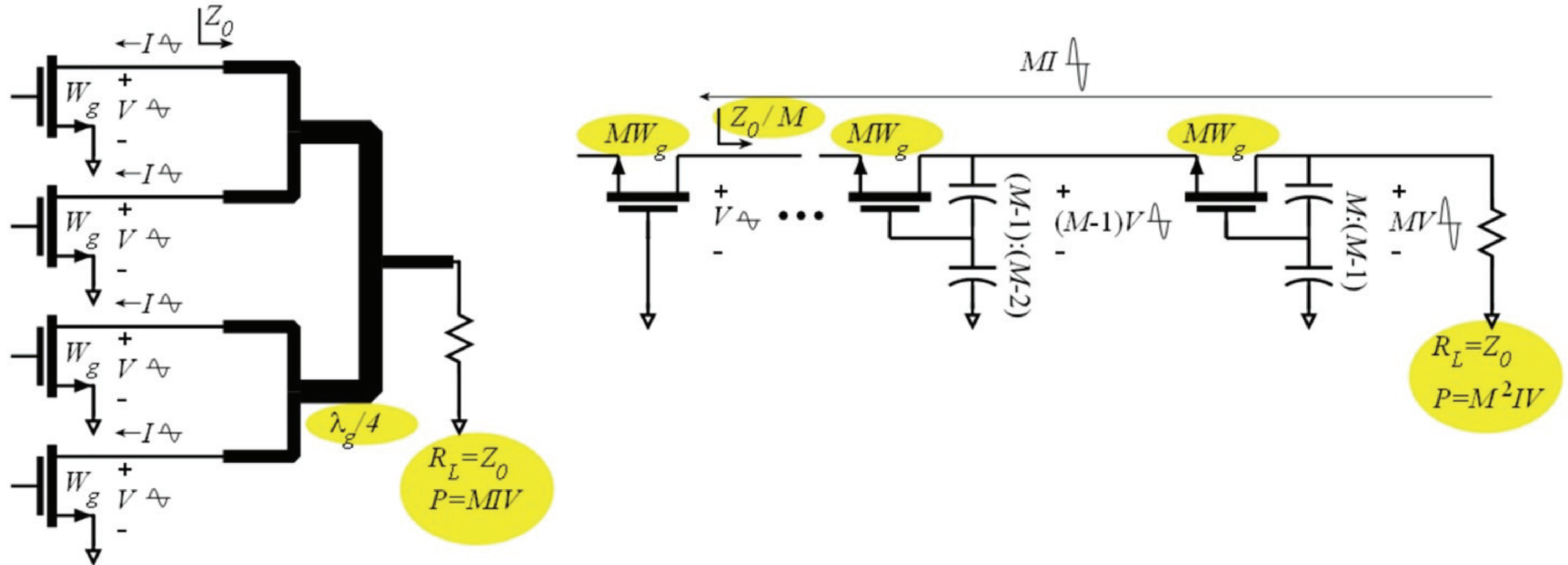
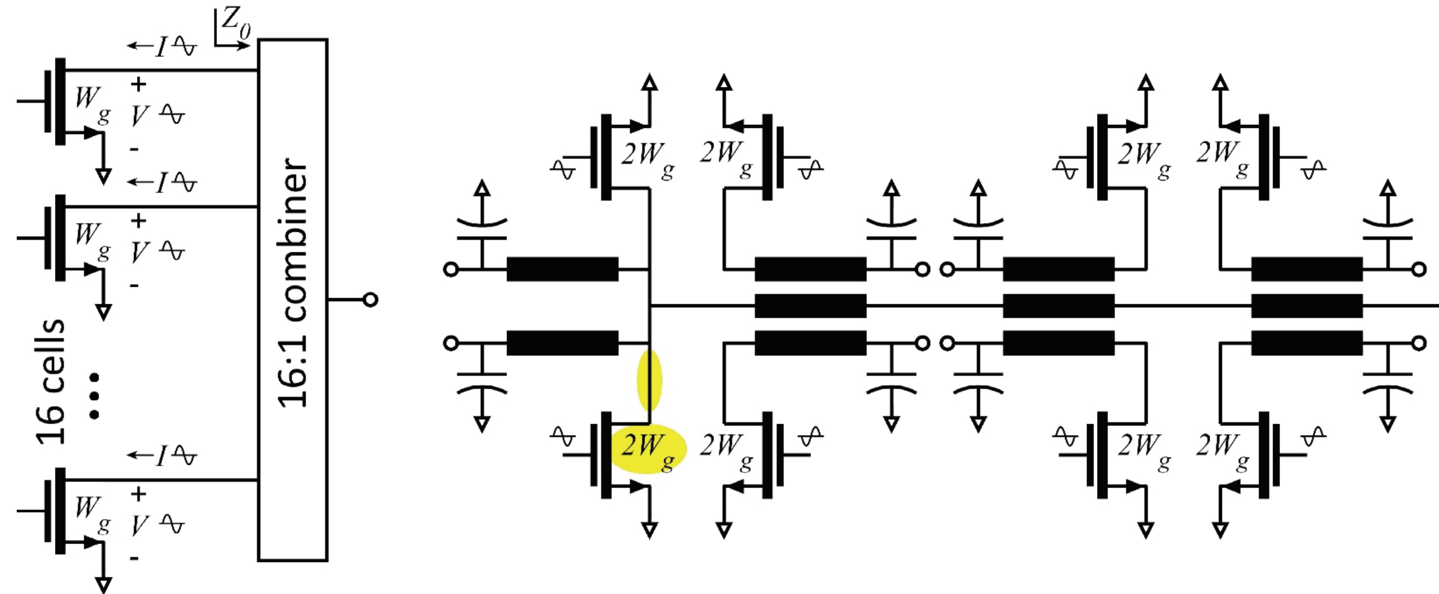
Transistor stacking. Why ? Why not ?



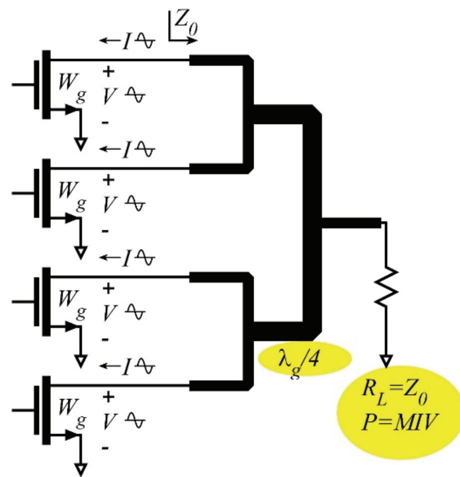
	Lower frequencies	Higher frequencies
Corporate combining	length $\propto 1/f \rightarrow$ large die area ✗ dB loss $\propto 1/\sqrt{f} \rightarrow$ high loss ✗	length $\propto 1/f \rightarrow$ small die area ✓ dB loss $\propto 1/\sqrt{f} \rightarrow$ low loss ✓
Series-connected	more transistor fingers per cell → ok ✓	more transistor fingers per cell→ parasitics ✗

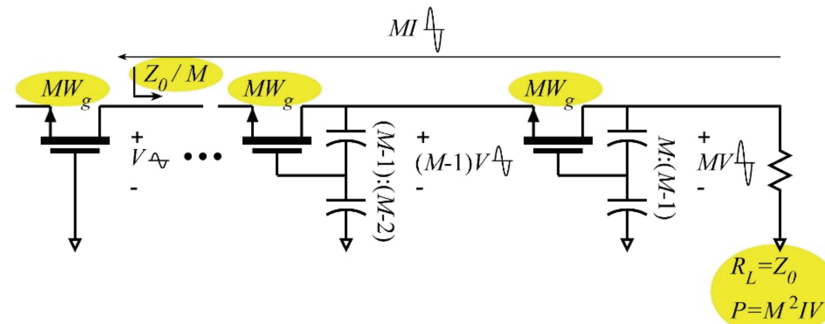
Sub-λ/4 Balun Combiners. Why ? Why not ?

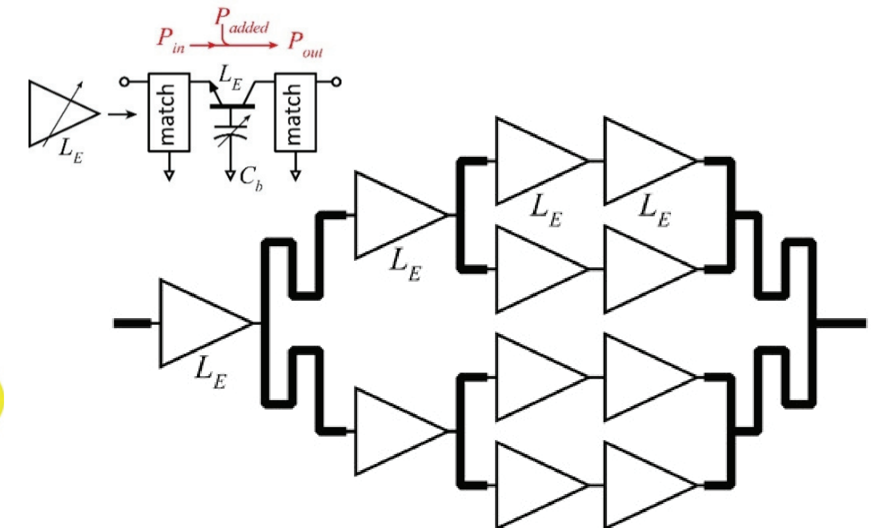


	Lower frequencies	Higher frequencies
Corporate combining	length $\propto 1/f \rightarrow$ large die area ✗ dB loss $\propto 1/\sqrt{f} \rightarrow$ high loss ✗	length $\propto 1/f \rightarrow$ small die area ✓ dB loss $\propto 1/\sqrt{f} \rightarrow$ low loss ✓
Sub-λ/4 Balun	more transistor fingers per cell → ok ✓	more transistor fingers per cell→ parasitics ✗ impedance shift of transistor-balun interconnect ✗

Cascade Combining: Why ? Why not ?





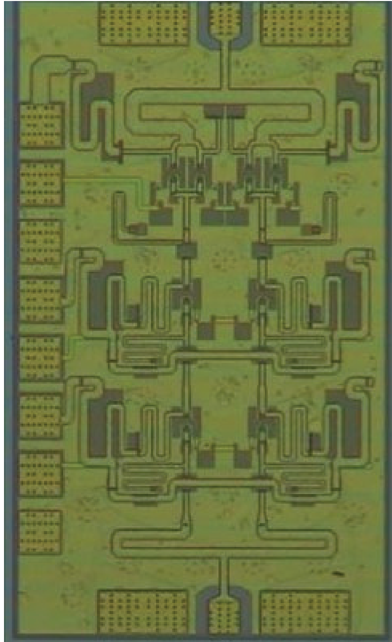


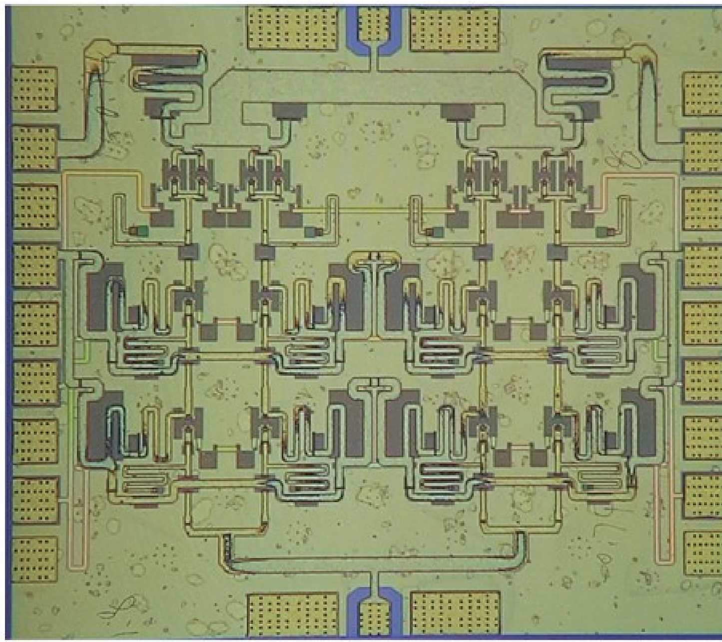
	Lower frequencies	Higher frequencies
Corporate combining	length ∝ $1/f$ → large die area ✗ dB loss ∝ $1/\sqrt{f}$ → high loss ✗	length ∝ $1/f$ → small die area ✓ dB loss ∝ $1/\sqrt{f}$ → low loss ✓
Series-connected	more transistor fingers per cell → ok ✓	more transistor fingers per cell → parasitics ✗
Cascade combining	large interstage matching networks ✗	small interstage matching networks ✓ small # transistor fingers per cell → ok ✓ cascade cell pass-though losses ✗

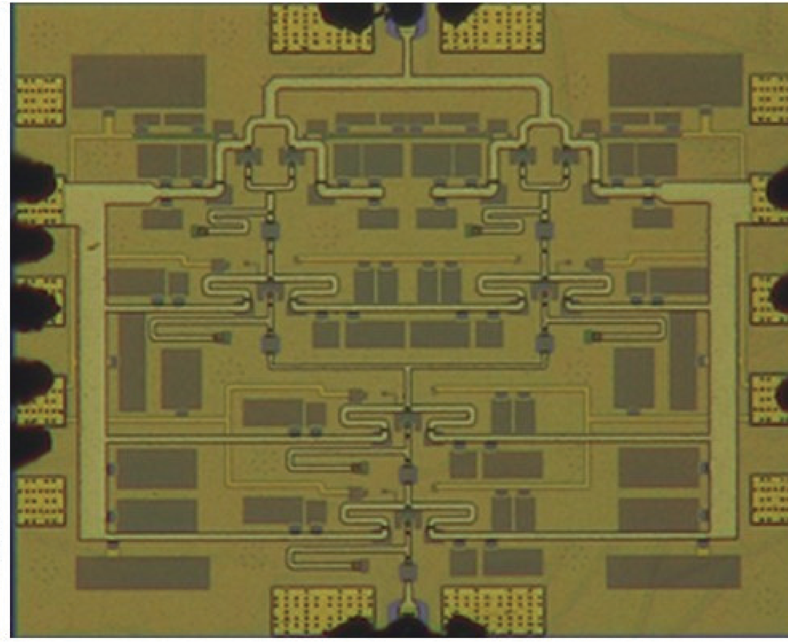
PAs with corporate & cascade combining

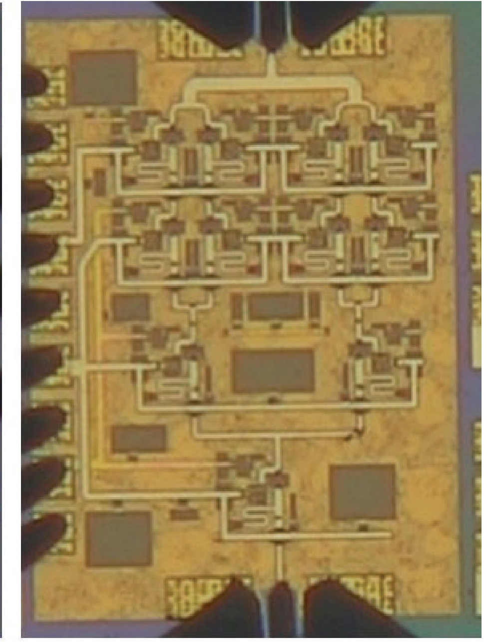
Teledyne 250nm InP HBT technology

Ahmed et al., 2020 IMS, 2020 EuMIC, 2021 IMS, 2021 RFIC







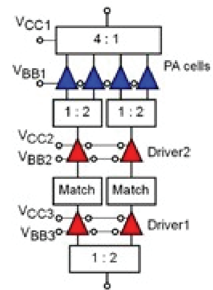


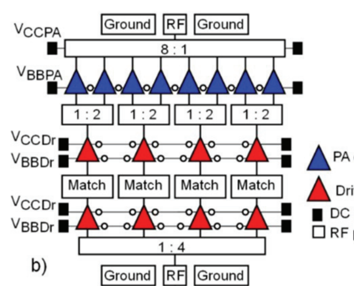
140GHz, 20.5dBm, 20.8% PAE

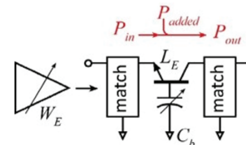
130GHz, 200mW, 17.8% PAE

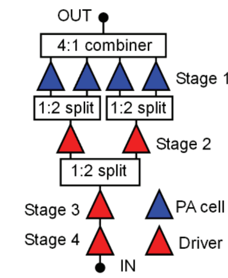
194GHz, 17.4dBm, 8.5% PAE

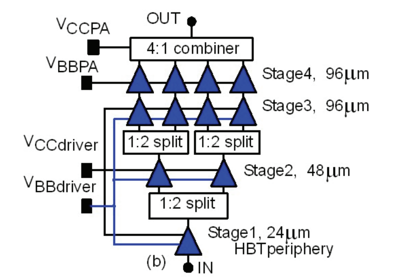
266GHz, 16.8dBm, 4.0% PAE











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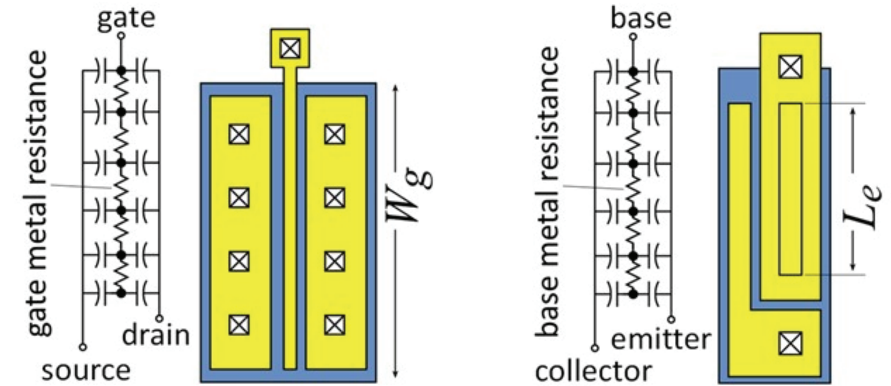
Current density, finger pitch limit cell output power

$$\text{Electrode } RC \text{ charging time} \propto (\text{finger length})^2$$

$$\text{Maximum finger length} \propto 1/\sqrt{\text{frequency}}$$

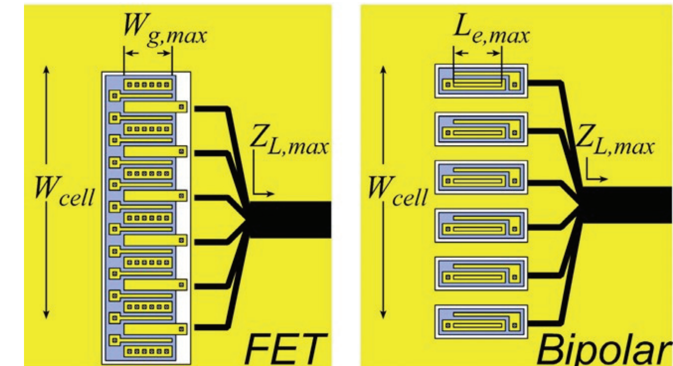
$$\text{Current per finger} \propto 1/\sqrt{\text{frequency}}$$



$$\text{Maximum cell width} \propto 1/\text{frequency}$$

$$\text{Maximum number fingers} \propto 1/\text{frequency}$$

$$\text{Maximum current per cell} \propto 1/\text{frequency}^{3/2}$$



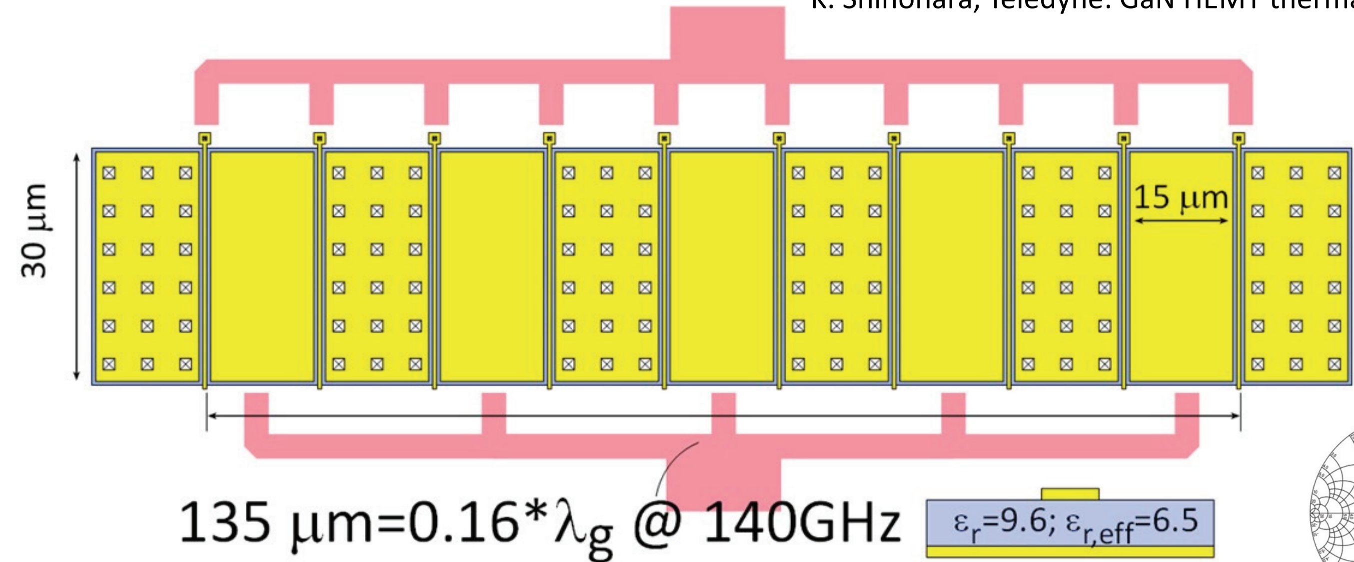
$$\text{Maximum RF power per cell} \propto (\text{maximum load resistance}) \cdot (\text{maximum current})^2 \propto 1/(\text{frequency})^3$$

$$\text{Compare to Johnson F.O.M.: maximum power per cell} \propto (\text{maximum voltage})^2 / (\text{minimum load resistance}) \propto 1/(\text{frequency})^2$$

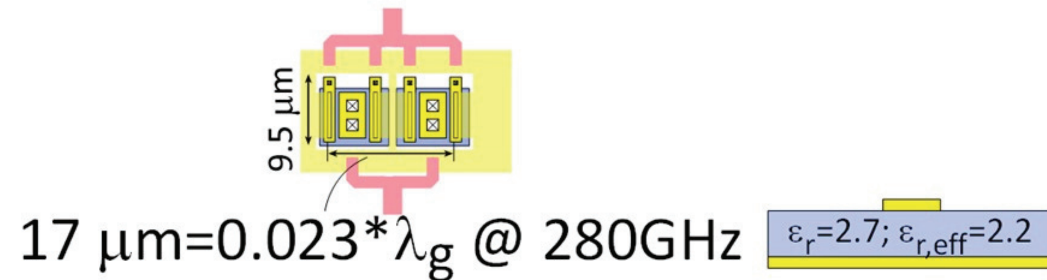
Current density, finger pitch limit cell output power

K. Shinohara, Teledyne: GaN HEMT thermal analysis

50Ω GaN PA cell @ 140GHz (1.6W)
25V swing, 1.67mA/μm,
gates: 30 μm width, 15 μm pitch



50Ω InP HBT PA cell @ 280GHz (40mW)
4V swing, 3.3mA/μm,
emitters: 6 μm length, 6 μm pitch



High V_{br}, low I_{max} ? Device sized to drive 50Ω might approach $\lambda_g/4$ width.
Small finger pitch is critical; limited by thermal design