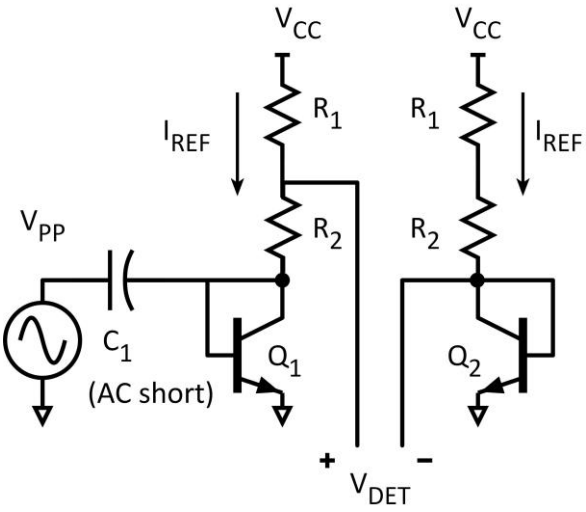
ECE 145C/218C second problem set: AGC loops

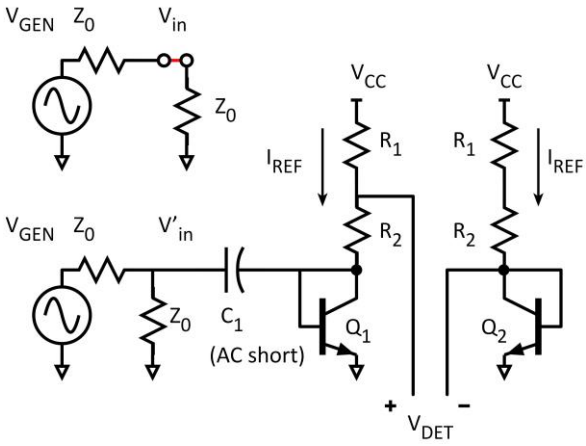
Problem 1: You will be working with the peak detector / power detector shown to the right. V_{CC} = 5V. Pick R1+R2 such that I_{REF} = 5 mA. Pick C_1 so that its capacitive reactance is less than 1 Ohm at 500 kHz. Let us *initially* pick R_2 =0 Ohms.



First, assume that the input is a *square wave*.

For Vpp=0.893 Volts, what value do you compute for V_{DET} ?

Problem 2: We now simulate using a sinusoidal signal and a generator a 50 Ohm output impedance. Continue to assume a signal frequency of 500 kHz . Note that a signal generator with a 50 Ohm output impedance will deliver half the open circuit voltage to a 50 Ohm load as the insect diagram indicates; $V_{in} = V_{GEN} / 2$. However once we include the loading of the peak detector the input voltage V'_{in} may or may not be equal to $V_{GEN} / 2$.



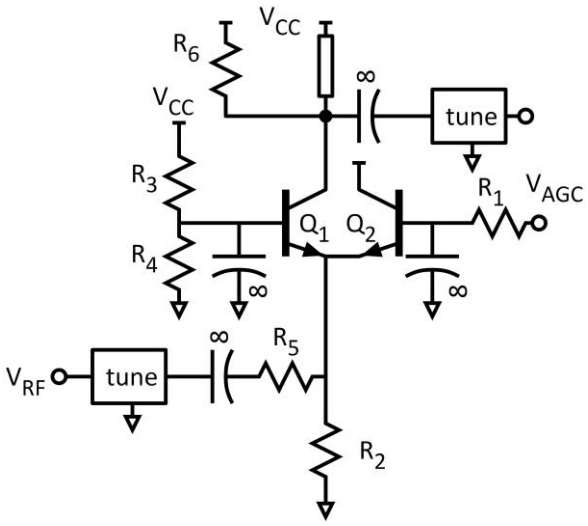
It is however the relationship between V_{In} and V_{DET} That we are concerned about Not the relationship between V'_{in} and V_{DET}.

Using a harmonic balance simulator from ADS and sweeping the available power from the generator, with Q1 and Q2 using MRF901 transistor models, simulate the relationship between the available power from the generator and the DC voltage. Provide this graph in your homework solution

Note carefully the value of this voltage at 3 dBm available power .

Problem 3: Now, keeping the value of $R_1 + R_2$ the same as the previous problems, Increase R_2 until V_{DET} is zero when the available power from the generator is 3 dBm.

Problem 3: You will now design and simulate a 915 MHz variable gain amplifier in ADS. Use mrf901 transistors. V_{CC} =5V. Select R3 and R4 such that the base of Q1 is biased at 2.5V and such that the current through R4 is 1 mA. Pick R_2 such that it carries 5 mA. Initially simulate with V_{AGC} =2.0V. Set R_1 = 1kOhm. Please initially set $R_6 = \infty$ Ohms and R_5 = 0 Ohms; you can choose to change these values if that makes design easier, but to do so will reduce the gain.



Design the output tuning network to provide a loadline match as this will provide the largest saturated output power. Design the input tuning network to provide a small signal match as this will provide the largest gain.

Make plots of the resulting s parameters over the frequency range from 800 to 1000 MHz. Make plots of input available power from the generator and output power delivered to a 50 Ohm load at 915 MHz signal frequency.

Problem 4: With V_{AGC} =2.0 V, the DC current in R_2 will pass entirely through Q1, with no current carried in Q2. As V_{AGC} is increased, a greater fraction of the current will be carried in Q2, and a lesser fraction in Q1. This will reduce the circuit gain. The distribution of currents between the two transistors will switch very quickly as V_{AGC} is varied, with almost all of the current in Q1 for V_{AGC} =2.5V - 52 mV and with almost all of the current in Q2 for V_{AGC} =2.5V + 52 mV. This is a rapid and nonlinear variation. However the variation in gain as a function of I_{C1} will however be relatively smooth and slowly varying.

Please make a graph of the dB magnitude of S21 as a function of I_{C1} . Please also make a graph of the dB magnitude of S twenty one as a function of V_{AGC}

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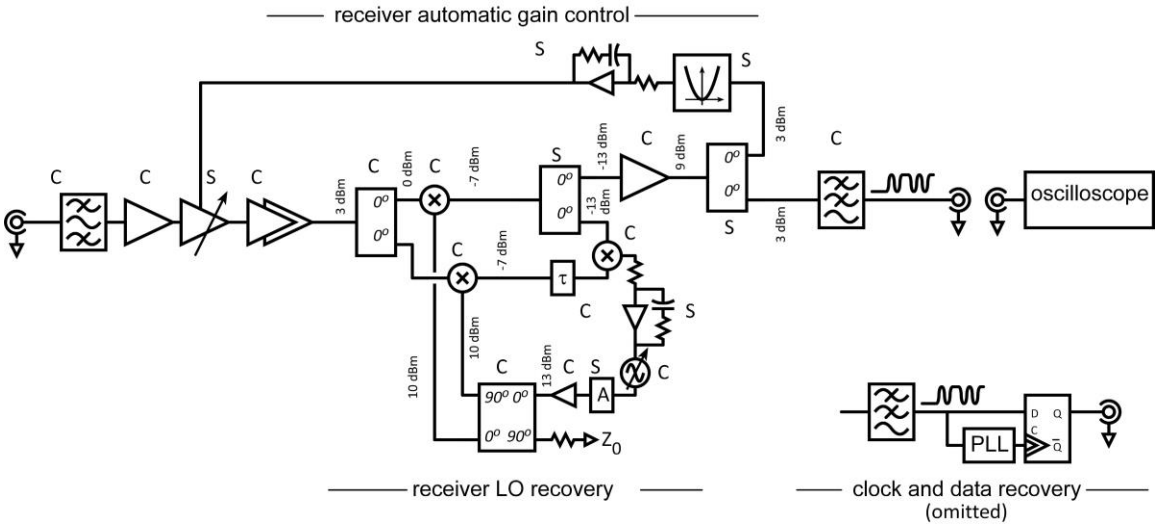
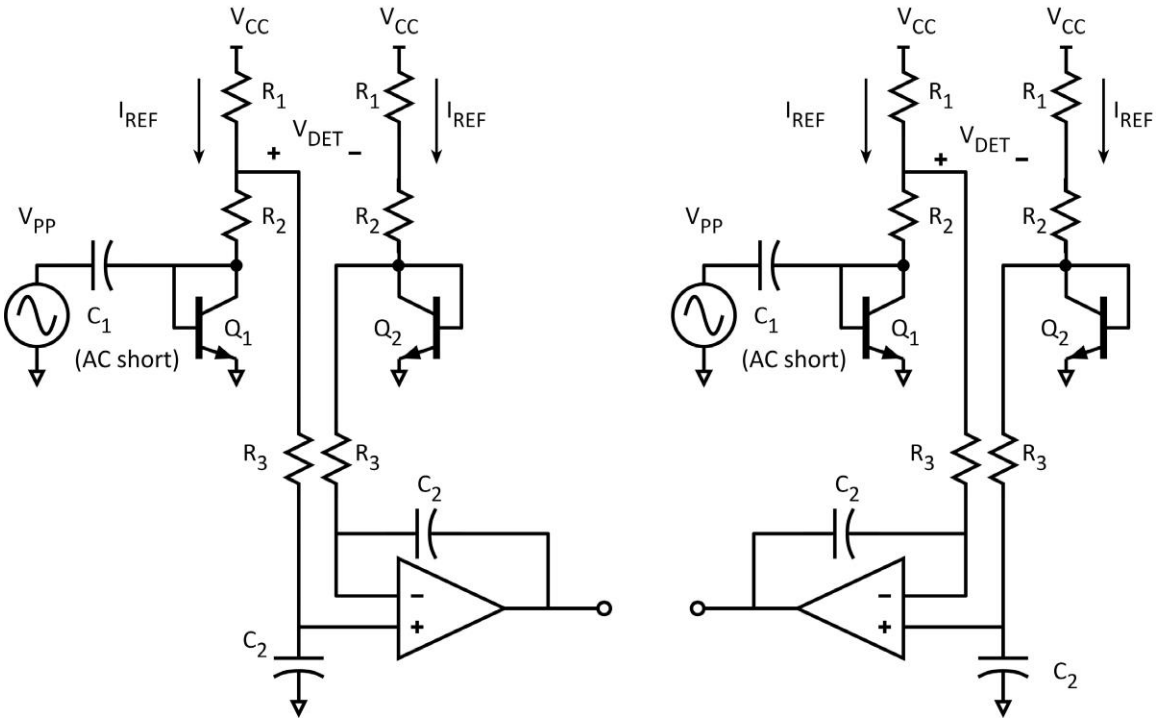
The above exercises in this problem set are to help you design the AGC loop for the receiver lab project. For your reference, the images below show some preliminary suggested signal power levels within the receiver, together with some block diagrams of what the AGC control loop might look like inclusive of the op amp feedback amplifier.


receiver automatic gain control
oscilloscope
receiver LO recovery
clock and data recovery
(omitted)
PLL
3 dBm
0 dBm
-7 dBm
-13 dBm
9 dBm
10 dBm
13 dBm
A
Z_0


V_{CC}
I_{REF}
R_1
R_2
R_3
V_{DET}
V_{PP}
C_1
(AC short)
Q_1
Q_2
C_2